NASA CONTRACTOR REPORT

NASA CR-1225

NASA CR-1225

INVERTER-CONVERTER AUTOMATIC PARALLELING AND PROTECTION

by C. L. Doughman, B. A. Marino, and N. D. Lenhart

Prepared by
WESTINGHOUSE ELECTRIC CORPORATION
Lima, Ohio
for Lewis Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • FEBRUARY 1969

NASA CR-1225

INVERTER-CONVERTER AUTOMATIC PARALLELING AND PROTECTION

By C. L. Doughman, B. A. Marino, and N. D. Lenhart

Prepared under Contract No. NAS 3-2792 by
WESTINGHOUSE ELECTRIC CORPORATION
Lima, Ohio

for Lewis Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – CFSTI price $3.00

ABSTRACT

Electrical control and protection circuits are developed for a multi-channel, paralleled ac system and for a multi-channeled, paralleled dc system. Electrical control for each of the two systems consists of automatic paralleling circuits and electrical contactor control circuits. Protection circuits for the ac system include overvoltage, undervoltage, overfrequency, underfrequency, frequency reference protection, overcurrent, load division and differential current. Protection circuits for the dc system are the same as for the ac system except that no frequency protection circuits are included. Test results verify and demonstrate the developed technology.

PREFACE

The work described herein was done at the Aerospace Electrical Division, Westinghouse Electric Corporation, under NASA Contract NAS 3-2792. Mr. Francis Gourash, Space Power Systems Division, NASA-Lewis Research Center, was the Project Manager for NASA. The entire program, "Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials," is described in five reports:

"Inverter-Converter Parallel Operation" defines and experimentally verifies the circuit conditions that must exist for operating static inverters and static converters in parallel (NASA CR-1224).

"Inverter-Converter Automatic Paralleling and Protection" defines and experimentally verifies the electrical control and protection circuits necessary for isolating faulted inverters and converters from a parallel system while maintaining continuity of high-quality electric power to load equipment (NASA CR-1225).

"Evaluation of Magnetic Materials for Static Inverters and Converters" defines the magnetic characteristics of improved materials for magnetic components as applied in advanced static inverters or static converters (NASA CR-1226).

"Load Programmers, Static Switches, and Annunciator for Inverters and Converters" assesses the characteristics of static electrical switches for both ac and dc systems, defines the characteristics of a load programmer for maintaining power to the critical system loads, and provides an annunciator function for displaying inverter and/or converter operating conditions (NASA CR-72454).

"Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials" is the summary report (NASA CR-72455).

Page Intentionally Left Blank

CONTENTS

CONTENTS (Cont.)

INVERTER-CONVERTER AUTOMATIC PARALLELING AND PROTECTION

by C.L. Doughman, B.A. Marino, N.D. Lenhart

SUMMARY

One approach for increasing the electric power capacity of a static conversion system is to operate inverters or converters electrically in parallel. NASA CR-1224 presents the theory and circuit techniques required to operate inverters or converters in parallel.

Once the technology for paralleling inverters and converters is developed, the next consideration is the development of practical circuit techniques for controlling and protecting these inverters or converters in a paralleled electrical system. The purpose of this report is to present the results of such development.

Electrical control and protection circuits are developed for a multi-channel, paralleled ac system and for a multi-channel, paralleled dc system. The ac system consists of several static inverters which convert dc power into multi-phase ac power. The dc system consists of several converters which increase dc power to a higher voltage level.

Electrical control for each of the two systems consists of automatic paralleling circuits and electrical-contactor control circuits.

Protection circuits for the ac system include overvoltage, undervoltage, overfrequency, underfrequency, frequency reference protection, overcurrent load division and differential current.

Protection circuits for the dc system include all protection listed for the ac system except that no overfrequency and underfrequency circuits are included.

Test results are discussed for both a two-channel, 400-Hz, ac system and a two-channel dc system to demonstrate the developed technology for future space applications.

INTRODUCTION

As space missions become more complex and increase in scope and duration, the required magnitude of electric power will increase. This increasing electric power requirement can be met by developing larger static inversion equipment for converting dc power into multi-phase ac power or into higher voltage dc power.

An alternate and more practical approach for obtaining higher power systems is to operate inverters or converters in parallel redundant systems. In this way, higher power level systems can be constructed using state-of-the-art inverters or converters. The resulting parallel system can be more reliable and has greater flexibility than a single inverter or converter system or a standby-redundant-system of the same rating.

This use of multiple systems operating electrically in parallel has been common in aircraft power systems where rotating generators develop the required electric power. Hence, many of the philosophies and techniques developed for aircraft systems can be extended to static conversion equipment for space missions.

Numerous developments of static inverters have resulted in circuit concepts that can be applied to space applications (refs. 1 and 2).

The purpose of the work described herein has been to extend the control and protection concepts for paralleled power generation systems to static-inverter or static-converter systems.

A static inverter is a device which transforms dc power to multi-phase (usually three-phase) ac power. A static converter is a device which transforms dc power of one voltage level to dc power of another voltage level (usually higher).

The main objective of the work described in this report is to develop the automatic control and protection circuits for a parallel system consisting of several inverters or converters and for the interconnecting distribution system necessary to provide power to utilization equipment.

A power system can be described as a group of subsystems interconnected to provide power to the utilization equipment as illustrated in figure 1. A subsystem consists of an inverter or a converter, a feeder system with contactors, and load

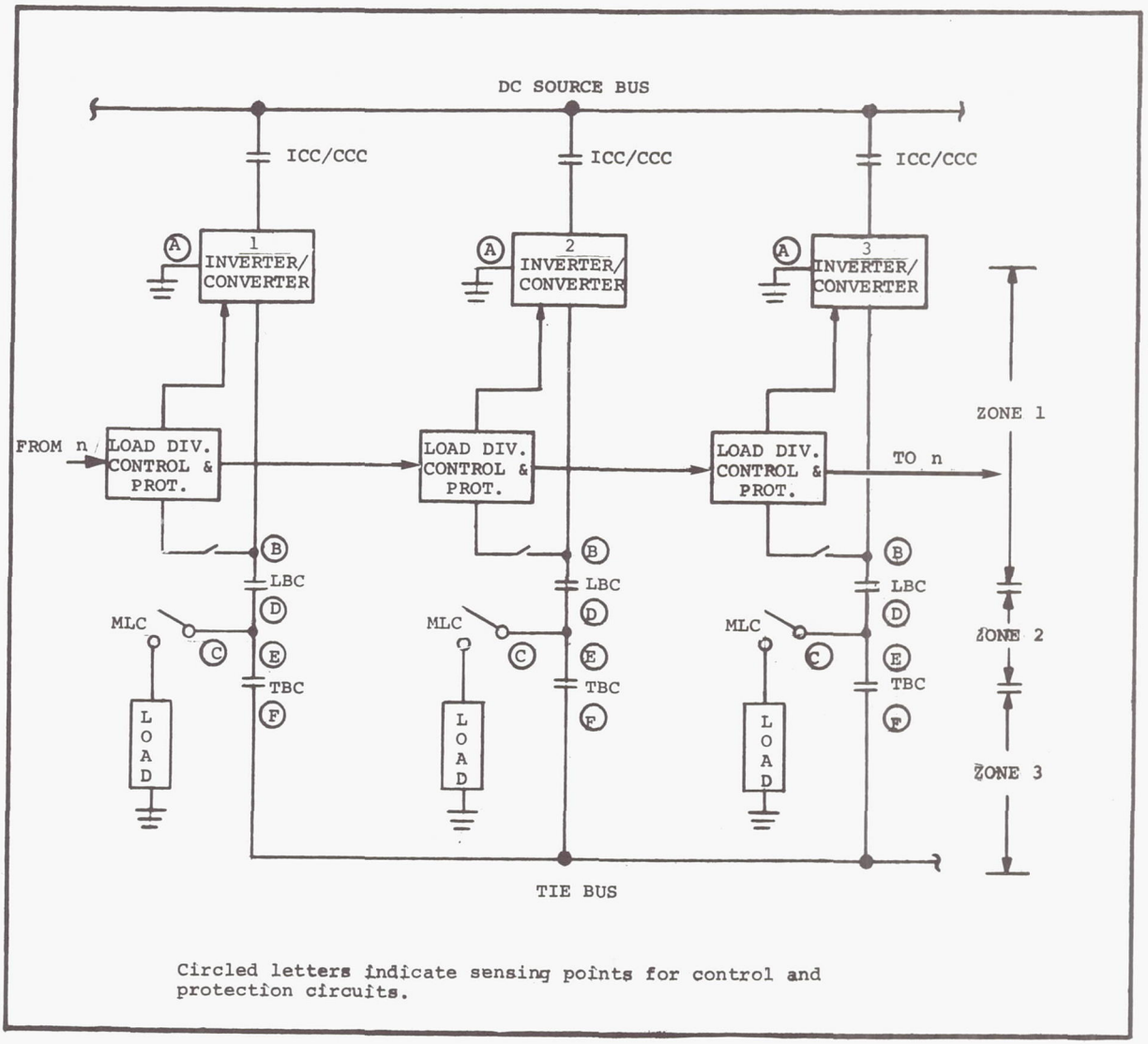


Figure 1. - Parallel System Line Diagrams

or utilization busses. Since the system under investigation is a parallel system, the means of interconnection between subsystems is provided by the tie bus. The tie bus provides a current path so that each inverter or converter supplies only its share of the total system load.

The zones indicated in figure 1 are used later in the description of faults in the distribution system of a parallel system. The circled lettered points in figure 1 indicate various sensing points for voltage, current, or frequency monitoring circuits used in the control and protection circuits.

The control functions consist of starting an inverter or converter, monitoring the power quality, connecting it to the load bus, paralleling it to the tie bus, and interconnecting the load-division circuits. The protection function consists of overcurrent protection for various portions of the distribution system, power quality protection, and load-division protection.

Table I describes the characteristics of the inverters and converters for which the breadboard control and protection circuits were designed.

Table I. - Characteristics of Power Sources Used in This Study

	INVERTER	CONVERTER
Input:		
Voltage	28 ±3 volts	28 ±3 volts
Current	0 to 45 amperes	0 to 45 amperes
Output:		
Capacity	750 volt-amperes	746 watts
Frequency	400 Hz ±0.1%	direct current
Voltage	120/208 wye, ±3%	153 volts, ±3%
Current (Steady State)	2.18 amps/phase	4.88 amps
Current (Fault)	4.4 amps	10 amps
Current Division (Paralleled)	10% of rated current	10% of rated current
Recovery Time:		
Application and Removal of Full Load (See Appendix A)	70 milliseconds	70 milliseconds

SYMBOLS

INVERTER	CONVERTER	
ICS	CCS	Control Switch
ICC	CCC	Control Contactor
INV OCP	COCP	Overcurrent Protection
LOAD OCP	--	Load Bus Overcurrent
---	TBOC	Tie Bus Overcurrent
---	AP	Auto-Paralleling
---	DTB	Dead Tie Bus
OF	--	Overfrequency
UF	--	Underfrequency
FRP	--	Frequency Reference Protection
MOS	MOS	Manual Override Switch
OV	OV	Overvoltage
UV	UV	Undervoltage
DP	DP	Differential Protection
LDP	LDP	Load Division Protection
LDC	LDC	Load Division Control
TD	TD	Time Delay
LBC	LBC	Load Bus Contactor
TBC	TBC	Tie Bus Contactor
SUSS	--	Start-up Synchronizing Signal
SYNC	--	Synchronizing Signal Between Inverters
MLC	MLC	Manual Load Control

CONTROL AND PROTECTION FOR PARALLELED STATIC INVERTERS AND CONVERTERS

Philosophy of Control and Protection

The purpose of an electric power system is to supply power to a load. Many malfunctions of individual system components or system faults may occur which could prevent system operation. Therefore, the system must be designed to supply power even though a number of system failures occur. Simply stated, the electric power system must be reliable. The definition of reliability, as it applies to a system design, is the probability that the system will perform its functions (1) within specified limits; (2) for a specified period of time; and (3) under specified operating conditions.

In considering the basic design for system applications, the system functions must be defined and the ground rules must be established. Limits of normal and abnormal operation must be established and the necessary protection for the

system must be determined. Since the period of operation and the operating conditions are influenced primarily by the individual application, these specifications do not affect the basic system philosophy but rather only the detailed design of individual system components.

Any electric power system can be considered to consist of two parts: (1) the power source with its associated control circuits that act to maintain the output power within specified limits; and (2) the load and distribution network. Since both parts are susceptible to malfunction or failure, the effect on system operation of failures in either of these areas must be considered and a means to maintain basic system requirements must be provided.

If the system consisted of only one power source, a power source failure would result in loss of the entire electrical system. However, if multiple power sources are provided, the failure of one source will not cause a failure of the entire system. From this, two criteria result:

(1) The total power capacity of an electric power system shall consist of a number of power sources.

(2) The system load shall be supplied even with the loss of some of the power sources.

This can be extended to cover the system loads. If the total system load were supplied from a common point, a failure at this point would appear as a total load fault and result in the loss of the entire system load. However, if the total system load consisted of a number of smaller loads that could be isolated should a failure occur on one, the remaining loads would not be affected. A third criterion for system operation is thus established.

(3) The total system load shall consist of a number of individual load connection points (load busses).

This is accomplished by providing system protection capable of selective isolation of the faulted area while maintaining maximum system load capability.

It is necessary to define protection prior to determining detailed requirements for normal operation. System protection is intended to prevent sustained abnormal or excessive transient conditions that may result in damage to, or malfunction of, either system utilization equipment or power sources. System protection is provided for abnormal system voltages, currents,

and (for ac systems) frequencies. Although system protection will not adjust or regulate the basic system parameters, it will monitor system parameters and isolate a faulted portion of the system after providing time for corrective action to occur. Corrective action is provided either by the power-source regulating circuits or by the load-bus secondary protection (fuses, thermal circuit breakers, and the like).

The protection consists of two types. The first type provides protection for system failures that occur during system operation, for example, abnormal voltage protection. This protection will prevent sustained abnormal voltage conditions.

The second type of protection prevents operation of the system until certain conditions are satisfied, thus avoiding occurrence of abnormal conditions. An example is the automatic paralleling of two power sources only when specific output power conditions are satisfied. If the two sources were allowed to parallel without satisfying certain conditions, possible damage to, or failure of, the entire system could result. From this, the fourth basic criterion for system operation is established.

(4) System protection shall isolate system faults before damage occurs to any other portion of the system while maintaining maximum load capacity.

Thus, the entire electric power system consists of a number of subsystems, each containing a power source, a portion of the total electrical load, and the required protection necessary to selectively isolate the faulted portion while maintaining maximum system load capacity. Figure 1 is a line diagram of such a system.

Approach to Control and Protection

In any electric power system, the basic system parameters of voltage, current, and (for ac systems) frequency are maintained within certain limits to assure compatibility between the system power sources and utilization equipment. A sustained variation of the system parameters outside these limits is considered an abnormal condition. A discussion of the causes of abnormal conditions and the action required to provide the necessary protection follows.

Abnormal current conditions. - Abnormal current conditions can occur during either parallel or isolated system operation. For parallel system operation, abnormal current conditions can

be caused by a failure of the load-division control circuit within the power source, by faults in the distribution system, or by system overloads. Abnormal current conditions during isolated system operation occur because of a system fault or an overload condition. To provide reliable system operation that satisfies both the second and fourth system operating criteria, protection must be provided for the following conditions.

Failure of the load-division control circuit. - Parallel system operation requires that the system load be divided among the power sources in proportion to their volt-ampere rating. Circuits have been developed to adjust the internal voltages of the power sources to force equal load division among the paralleled units (NASA CR-1224). It was determined that the load division between paralleled inverters or converters could be maintained within 10 percent of their nominal rating (0.22 amperes per phase for the test inverters, and 0.5 amperes for the test converters). System protection is required to provide corrective action if a load-division control circuit fails. Since the load unbalance is a result of a failure in the load division control circuit, the load division protection circuit isolates the subsystem from the remainder of the system. The subsystem is then operated as an isolated system supplying its own load.

Load unbalance among the paralleled units can occur as either a transient or steady-state condition. When large system loads are applied or when power sources with various loads are paralleled, load unbalance will occur for short periods. These unbalances are caused not by failure of the load-division control circuits but by inherent characteristics of the load-division control circuits. These conditions will not affect the system operation nor result in malfunction of the power source. The transient response of the load-division control circuits was determined from load-division tests to be less than 70 milliseconds. These data are shown in the appendix.

To prevent nuisance operation of system protection, the load-division protection circuits must be compatible with the transient-response characteristics of the load-division control circuits. This is accomplished by providing a time delay that is initiated by the load-division protection circuit. This time delay must be longer than the transient response of the load-division control circuits but shorter than the maximum overload capability of the power sources themselves.

The load-division protection circuit must also be compatible with the overload capability of the power source. The maximum

overload capacity was chosen as 120 percent to be compatible with the overload rating of the power source and to provide a reasonable safety margin.

Summarizing, the load-division protection must operate when the load unbalance among paralleled power sources exceeds 10 to 20 percent of their rated load for a period greater than the time delay. If the current unbalance persists beyond the time delay, the tie bus contactor is tripped isolating the subsystem from the tie bus.

Parallel system overcurrent faults. - During parallel system operation, feeder faults may occur anywhere within the system. To aid in determining the location of a fault, the parallel system is divided into three zones. The fault protection is intended to protect only the power sources and the distribution network and not the individual loads connected to the subsystem load buses. The protection for these individual loads must be provided by secondary protection which consists of thermal circuit breakers, current limiters, or fuses. The fault and overload characteristics of these devices closely match those of the individual loads and provide selective fault isolation for individual load faults.

Zone 1 includes the power source and the distribution feeders up to the load-bus contactor (figure 1). The protection provided within this zone is intended to protect against feeder faults that occur on the output of the power source. This output extends to the load-bus contactor since this is the first point at which the power source can be isolated from the system. No secondary protection for clearing a fault is provided within Zone 1; hence, coordination of fault protection is not necessary. The Zone 1 fault is isolated from the entire system and the load bus can be connected to the system through the tie bus.

The protection provided for faults occurring within Zone 1 de-energizes the power source and trips the load bus contactor. No time delay other than that inherent within the protection circuit is required.

Zone 2 includes the subsystem load bus and the distribution system between the load-bus contactor and the tie-bus contactor (figure 1). During parallel system operation, faults that occur within this zone are supplied by both the subsystem power source and all other subsystems connected to the system tie bus. A fault within this zone is a result of a fault on either the subsystem load bus that will be cleared by the secondary protection provided for individual loads or a feeder fault that will not be cleared by the secondary protection. The system protection provided for this zone must distinguish between these two types of

faults. A time delay provides time for the secondary protection within the load bus to clear the fault, thus providing the necessary protection and coordination.

Faults occurring in Zone 2 and persisting beyond the time delay must be isolated from both the power source and the system tie bus by tripping the tie-bus contactor and load-bus contactor.

Zone 3, for each subsystem, includes the entire system beyond the tie bus contactor (figure 1). A fault occurring in Zone 3 appears as a tie-bus fault for each subsystem, although the fault may actually occur within Zone 1 or Zone 2 of any other subsystem.

For faults occurring on the system tie bus, the Zone 3 fault protection of each subsystem must isolate each subsystem from the system tie bus. For faults that occur within Zones 1 or 2 of another subsystem, the tie-bus fault protection of the unfaulted subsystems must coordinate with the Zone 1 or Zone 2 protection of the faulted subsystem to allow sufficient time to isolate the fault without isolating all systems from the tie bus. Time delays provide the necessary coordination. The lengths of the time delays are sufficient to allow the secondary protection for the individual loads on any subsystem to clear the fault.

For faults occurring in Zone 3 of each subsystem, the fault protection coordinates with Zone 1 and Zone 2 protection of other subsystems to allow removal of faults within these zones prior to isolation of the subsystem from the tie bus by tripping the tie-bus contactor.

Isolated system overcurrent faults. - During isolated system operation only Zone 1 and Zone 2, as defined above, exist. The protection provided during parallel system operation for these two zones is also provided during isolated system operation.

Abnormal voltage conditions. - Abnormal voltage conditions can occur for either isolated or parallel system operation. For parallel system operation, abnormal voltage conditions result in an unbalance in load division between paralleled units. The result of this unbalance is an abnormal current condition, which was discussed under the load-division fault. For isolated system operation, abnormal voltage conditions can occur as either transient or continuous undervoltage or overvoltage conditions, and abnormal voltage protection must be provided for the system.

Transient voltage conditions exceeding the nominal system voltage are caused by the sudden application or removal of system loads or faults. The transient is short and is characteristic of the regulating circuit in the power source.

To provide system protection and to prevent nuisance operations of the abnormal voltage protection, a means is required to distinguish between the normal system transient conditions and the abnormal system voltage conditions. This is accomplished by a time delay of a duration compatible with the voltage-time characteristics of both the power source and the utilization equipment.

Generally, the overvoltage time delay has an inverse time-voltage characteristic while the undervoltage time delay is fixed. The inverse time-voltage characteristic of the overvoltage circuit is used to provide maximum protection for the utilization equipment. The length of the time delay is determined by the magnitude of the overvoltage conditions. No inverse time delay is provided in these protection circuits because the volt-time limits of the utilization equipment are not specified and because the protective features of the circuits can be demonstrated equally with a fixed time delay. This also simplifies the breadboard demonstration system since the same time delay can be used for overvoltage and undervoltage as well as overfrequency and underfrequency faults.

An abnormal voltage condition occurring during isolated system operation results from a failure in the voltage regulating circuits and requires the power source to be isolated from the subsystem load bus and de-energized.

Abnormal frequency conditions. - Abnormal frequency conditions can occur anytime after startup during both isolated and parallel system operation. Those occurring during parallel system operation are the most dangerous since the out-of-phase condition between paralleled inverters would cause large current variations in the parallel system. During startup of an inverter, protection must be provided against the possibility of the frequency never meeting the specified limits. A time delay, in the control and protection circuit, allows time for frequency to stabilize during startup. If the frequency is not normal at the end of the time delay or if the frequency goes out of limits during isolated operation, the inverter must be shut down. If the load bus is not faulted, it can be connected to the parallel system by closing the tie-bus contactor.

A second type of frequency fault is failure of the frequency reference. Because all paralleled inverters are synchronized from a single frequency reference, this type failure would instantly allow all paralleled inverters to run at their free-running oscillator frequency. The parallel system would not be a usable power source under this condition. Therefore, protection must be provided to switch from one frequency reference to another without disturbing the parallel system.

INVERTER CONTROL AND PROTECTION

Two modes of system operation for the inverter system are provided: automatic and manual. Although automatic is the normal mode, manual system operation is provided if the automatic mode fails.

A manual override switch, provided for each subsystem, selects the mode of system operation. Selection of either mode of operation for a subsystem prevents the other mode from operating. When the switch is placed in the AUTOmatic position, 28 volts dc is applied to the automatic control and protection circuits and to an inverter control switch. The subsystem is then ready for automatic operation. When the switch is placed in the MANual position, a ground circuit is provided for the trip and close coils of the inverter control contactor (ICC), the load bus contactor (LBC), and the tie-bus contactor (TBC) through manually operated switches. In the OFF position, neither automatic nor manual operation is provided. Figure 2 shows the connection of the necessary switches for both automatic and manual system operation.

Manual System Operation

Manual system operation, the secondary mode, provides a means of operating a subsystem independent of the automatic control and protection circuits. During manual system operation, the automatic control and protection circuits are not operative.

To operate the system manually, four switches are required in addition to the manual override switch (MOS). Figure 2 shows the connection of these switches. Switch S3 controls the inverter control contactor, S4 the load-bus contactor, and S5 the tie-bus contactor. Switches S4 and S5 also control the load-division control (LDC) circuit in the inverter by shorting the secondary winding of the LDC current transformer when the MOS is in the MANual position and either S4 or S5 is in the TRIP position.

The manual mode of system operation is selected by placing the MOS in the MANual position. The inverter is then energized by placing the ICC Manual Control Switch (S3) in the CLOSE position. After the inverter is started, it is connected to the subsystem load bus by placing the LBC Manual Control Switch (S4) in the CLOSE position. To connect the subsystem to the tie bus, the terminal voltage of the inverter must be in phase with, and of the same magnitude as, the inverters already connected to the tie bus. (Unless, of course, no other inverter is connected to the tie bus.) For these systems, the voltage may be within five percent of the rated value. The phase-angle difference between the

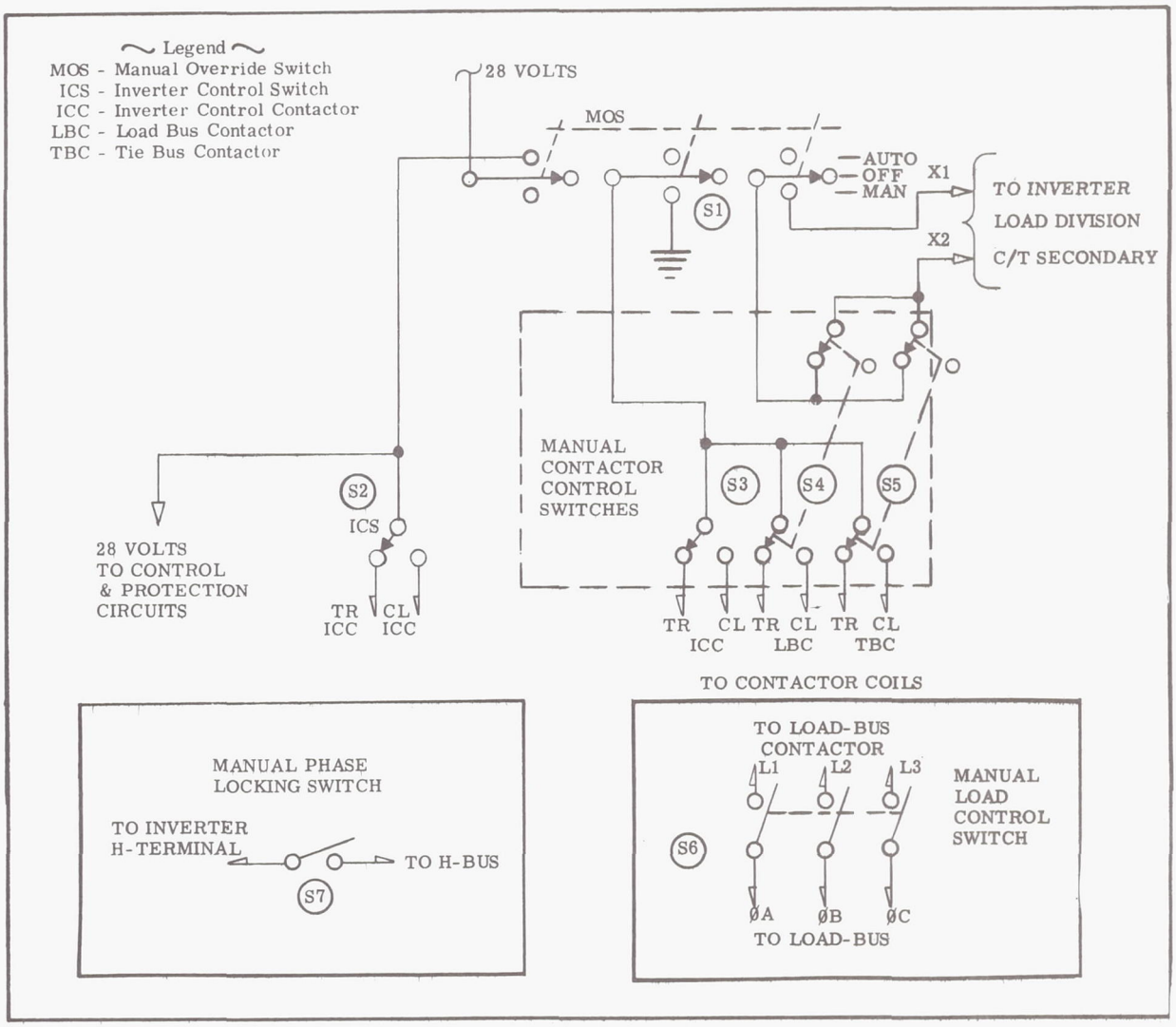


Figure 2. - Inverter-System Switch Connections For Automatic and Manual System Operation

terminal voltages should be within 10 to 15 degrees which is the natural phase displacement of the loaded and the unloaded inverters. To insure an in-phase condition, the Manual Phase Locking Switch (S7) is placed in the CLOSE position. This action ties the count-down circuits of the parallel inverters together such that each inverter's count-down circuit operates in phase. After assuring that the voltage is proper, the TBC Manual Control Switch (S5) is placed in the CLOSE position. Although the external automatic control and protective functions are inoperative, the voltage regulator and load-division control circuits, located within the inverter, are operative. Any contactor may be

operated manually and in any sequence with the inverters in the manual mode of operation. In addition, a manually operated switch (S6), is provided. Its purpose is to isolate the subsystem load bus from the system. This switch is referred to as the Manual Load Control Switch in figure 2. The Manual Load Control Switch can be operated during either automatic or manual system operation and is provided to allow a particular subsystem inverter to be connected to the system tie bus without supplying that subsystem load bus.

Development of Automatic Control and Protection Functions

Automatic system operation requires only one manual switch (ICS in figure 2) in addition to the Manual Override Switch. The function of the ICS is to connect dc power to the inverter by closing the Inverter Control Contactor. The rest of the startup procedure is performed automatically by the control and protection (C/P) circuits.

Automatic control of a parallel inverter system includes the assurance that conditions are proper for parallel operation before an inverter is paralleled to the system. The automatic protection circuits function to assure that these conditions prevail while an inverter is operating. The function of the protective circuits is not to restore a malfunctioning inverter subsystem to normal conditions but to isolate that portion of the subsystem from the parallel system which is not operating within the nominal limits prescribed for the system. The preceding section defines the general requirements and approach to protection as it applies to inverters operating in a parallel system. Figure 1 shows the layout of a parallel inverter system with the required sensing points indicated by circled letters A, B, and C. The present discussion integrates these elements into a control and protection network to determine the various normal and abnormal modes of system operation.

The control and protection requirements are first translated into a truth table which specifies a set of circumstances that must prevail before a desired action can occur. Circuit implementation is accomplished by providing the necessary sensing circuits to monitor system parameters and then providing the required logic circuits to meet the specifications generated by the truth table. The following discussion generates each column of the truth table (table II).

As stated above, there are two requirements for initiating inverter startup in the automatic mode of operation: the MOS must

Table II. - Truth Table for Inverter Control and Protection

Independent Variable		Column Number																		
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
		Initiate System Startup	Startup Fault				Normal Start			OV Fault	UV Fault	OF Fault	UF Fault	Zone 3 Fault	Zone 2 Fault		Zone 1 Fault	Load Division Fault	Manual Shutdown	Freq. Ref. Failure
A	MOS-AUTO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
B	ICS-CLOSE	1																		
C	ICS-TRIP		0	0	0	0														
D	OV		1				0			1								1		
E	UV			1			0				1									
F	OF				1		0					1								
G	UF					1							1							
H	TD1 (no power ready)		1	1	1	1														
I	LBC-CLOSE (memory)							1	1	1	1	1	1					1		
J	TD7 - initiated by I							1												
K	TBC-CLOSE (memory)								1									1		
L	ICC & LBC-TRIP (memory)						0													
M	TBC-TRIP (memory)		0	0	0	0		0		0	0	0	0				0			
N	TD2									1	1	1	1							
O	LDP																	1		
P	TD6 - initiated by 0																1			
Q	DP														1					
R	LOAD OCP														1					
S	TD5* - initiated by R													1		1				
U	INV OCP													1		ø				
V	TD4* } initiated by U															1				
W	TD3* }																			1
X	Tuning Fork Failure						0													
Y	LBC-TRIP (memory)																			
Z	Reset Trip Memories	0	0	0	0	0				0	0	0	0	0	0	0	0	0	ø	

* TDS < TD4 < TD3

Dependent Variable		Column Number																		
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
T1	ICC-CLOSE	1																		
T2	LBC-CLOSE & set memory						1													
T3	TBC-CLOSE & set memory		1	1	1	1		1		1	1	1	1				1			
T4	ICC-TRIP & set memory		1	1	1	1				1	1	1	1			ø	1		1	
T5	LBC-TRIP & set memory		ø	ø	ø	ø				1	1	1	1			1	1		1	
T6	TBC-TRIP & set memory													1	1			1	1	
T7	Load Division Control								1											
T8	Sync Bus Signal connected to Sync Bus								1											
T9	To H Bus								1											
T10	Switch to Tuning Fork No. 2																			1
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

LEGEND

1 - indicates that the condition must exist to perform the function.

0 - indicates that the condition must exist to perform the function.

ø - indicates that either 1 or 0 may exist (don't care condition).

(a)-T number is TRANSMISSION or action resulting from a specific combination of Independent Variables.

NOTES

1 - System Control and Protection is accomplished on a subsystem basis. Subsystem is considered paralleled when both LBC and TBC are closed.

2 - All functions reading horizontally are OR functions, while all functions reading vertically are AND functions.

3 - See Figure 4 for definition of other terms.

be in the AUTOmatic position and the ICS must be in the closed position. Column 1 of table II shows this condition which can be stated in symbolic form as

$$T1 = A \cdot B$$

After subsystem startup has been initiated, the output of the inverter remains zero for about five seconds. This time delay is a part of the inverter circuits. Because the output is zero for an extended time, the ICS must also initiate a time delay within the C/P circuits to allow time for normal startup. This time delay is identified as the no-power-ready time delay (TD1) and it provides 12 seconds for inverter startup. Time delay TD1 is controlled by two elements: (1) the position of the ICS and, (2) the quality of inverter output voltage. Power quality is monitored at point B of figure 1 by four circuits: overvoltage (OV), undervoltage (UV), overfrequency (OF), and underfrequency (UF). TD1 will continue to run until either the ICS is placed in the TRIP position or the power quality limits are met.

If a power-ready condition is not achieved within 12 seconds (columns 2, 3, 4, and 5 of table II), the no-power-ready time delay shuts down the inverter by tripping the inverter control contactor. Since the failure of inverter startup was not caused by the subsystem load bus, the load bus is connected to the parallel system by closing the tie-bus contactor. The inverter is now isolated from the system since the load-bus contactor has not been closed.

Alternately, if a power-ready condition is achieved within 12 seconds, the no-power-ready time delay is stopped. The load-bus contactor is closed because the abnormal voltage and frequency conditions have been removed (column 6). The subsystem is then operating as an isolated system. This is a temporary condition because the subsystem will immediately attempt to connect itself to the system tie bus.

The signal closing the LBC is put into a memory circuit since an abnormal voltage or frequency can remove this signal. The memory circuit is reset by a LBC-Trip signal. The LBC-Close memory signal initiates a time delay (TD7) which closes the TBC. TD7 ensures that before the inverter is paralleled to the system (column 7) no abnormal voltage or frequency condition is present and ensures that the distribution system is not faulted. The Load Division Control (LDC) circuit in the inverter should now be made operative (column 8). Both LBC and TBC must be closed to initiate the LDC circuit because this condition indicates that the inverter is paralleled. The inverter has now been started and paralleled to the system tie bus.

Satisfactory operation of paralleled inverters can be obtained only when three criteria are met: (1) the terminal voltages of the paralleled inverters are of the same frequency; (2) the terminal voltages of the inverters are in phase; and (3) the magnitudes of the terminal voltage of the paralleled inverters are equal. The first criterion of parallel operation is met by utilizing a common frequency reference for all the inverters (ref. 1). The third criterion for parallel operation is met by a voltage regulator with provisions for ensuring proper current division among the paralleled inverters. The synchronization requirements for parallel inverters, then, reduce to ensuring the proper phase relationship of the terminal voltages. This is accomplished by synchronizing the count-down circuits within each inverter with a pulse occurring once each cycle of the 400-Hz terminal voltage. This signal is generated primarily within each inverter countdown by a combinational logic circuit. This signal is controlled by the automatic control and protection circuits to apply an external sync signal to an inverter being paralleled to the system. Synchronization with the parallel system is accomplished during the inverter startup time delay by applying a sync signal at the H-terminal of the inverter. This terminal is identified in figure 3.

After the load-bus and tie-bus contactors have been closed, the inverter H-terminal is connected to the H bus (column 8). The H-terminals of the paralleled inverters must be interconnected to assure in-phase operation during fault conditions and normal load switching. The details of the design and the operation of the synchronization process are discussed later under "Inverter Control and Protection Circuit Design".

Once paralleled, the system continues to operate as a parallel system until an abnormal condition occurs. The appropriate system protection then removes or isolates the abnormal condition. The general requirements for subsystem protection are discussed in a preceding section "Approach to Control and Protection". This discussion is expanded, where necessary, to derive the remainder of the truth table.

For faults affecting power quality (abnormal voltage or frequency), a time delay is used which is long enough to ensure that normal switching transients do not cause false tripping. TD1 is too long to provide this function. Therefore, a shorter time delay (TD2) is used. To prevent premature shutdown of an inverter during startup, TD2 cannot be initiated until the LBC-Close memory circuit is activated (columns 9, 10, 11, and 12 of table II).

The time delays of the overcurrent protection circuits for Zones 2 and 3 provide two functions. First, the time delays allow time for the secondary protection (fuses, thermal circuit

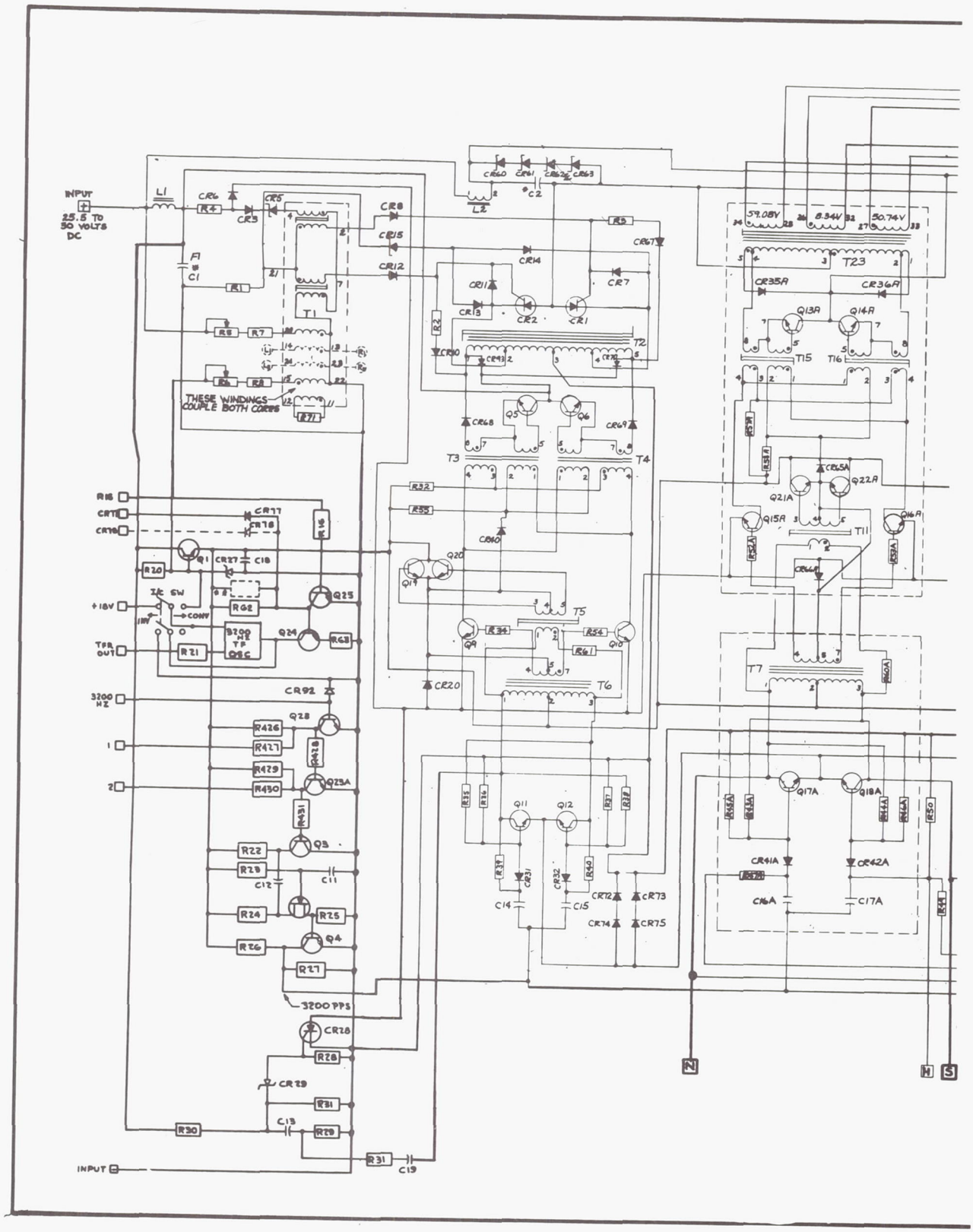
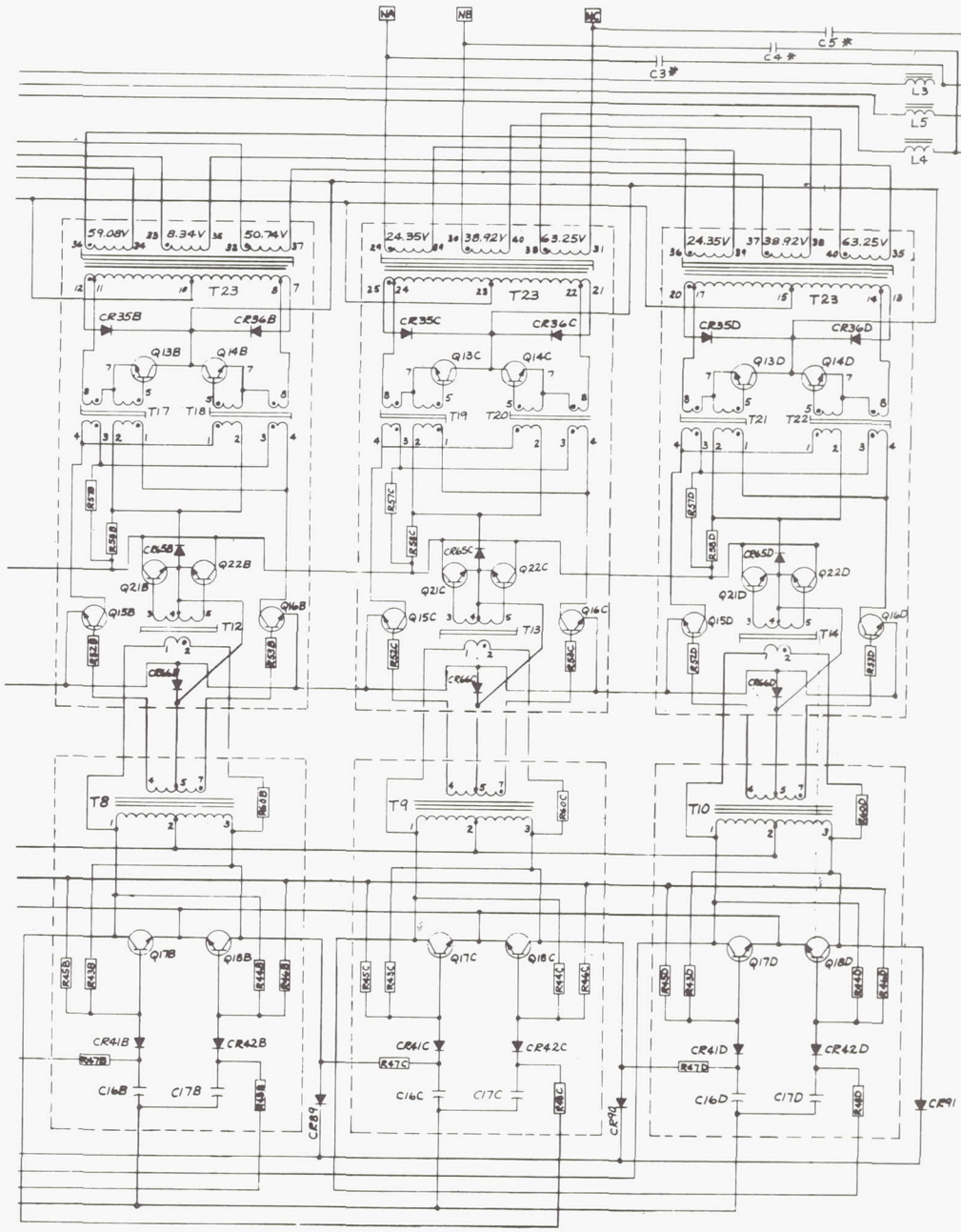


Figure 3. - Schematic Diagram of Inverter/Converter Models to be Used to Demonstrate Parallel Operation



* C1, C2, C3, C4 & C5 ARE PARALLEL CAPACITOR COMBINATIONS

** ADDITIONAL RESISTORS & DIODES ADDED WHEN MORE THAN TWO INVERTERS ARE OPERATED IN PARALLEL.

Figure 3. - Continued

(Con't from preceding page)

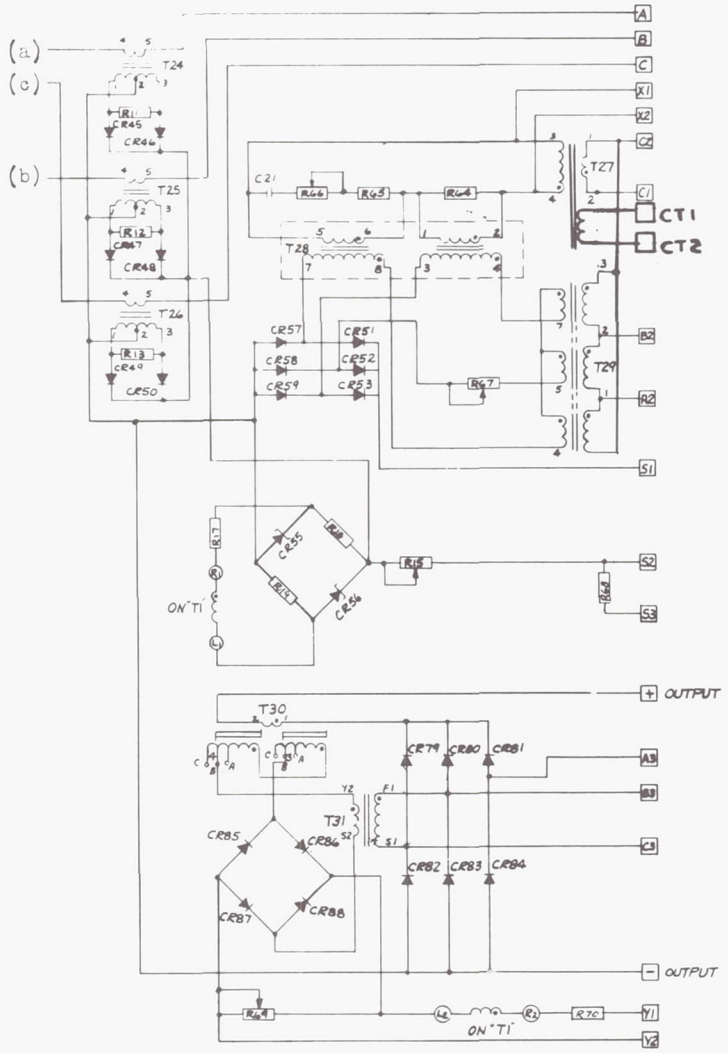


Figure 3. - Continued

breakers, and the like) to operate. Second, the time delays provide the necessary signals to differentiate between tie-bus and load-bus faults. Time delays TD3, TD4, and TD5 provide these signals. Load-bus overcurrent protection senses the total current to the load bus. If the load-bus current exceeds 125 percent of rated current, TD5 is initiated. The inverter overcurrent protection senses the output current of each phase of the inverter, and if any phase current exceeds 125 percent of rated current, TD3 and TD4 are initiated.

Overcurrent faults on the tie bus of a parallel system activate all the inverter overcurrent protection circuits. The inverter overcurrent protection senses inverter current at point B of figure 1. Time delays TD3 and TD4 are thus started on all subsystems. To determine the location of the fault, TD4 (the shorter of the two) trips the tie-bus contactor and TD3 trips the LBC. TD4 in each subsystem trips the TBC, thus isolating each subsystem from the tie bus (column 13 of table II). This removes the inverter overcurrent protection signal thus stopping TD3. Each subsystem now operates as an isolated system, i.e., each supplying power to its load bus.

Overcurrent faults occurring on a subsystem load bus (point C of figure 1) also initiate TD3 and TD4 because the inverter overcurrent protection circuit is activated. The subsystem with the faulted load bus also initiates TD5 through its load-bus overcurrent protection circuit. Since the remainder of the parallel system sees an apparent tie-bus overcurrent condition, TD5 must be of shorter duration than TD4 to remove the faulted subsystem from the tie bus (column 14). This sequence, therefore, removes the overcurrent condition, stopping TD3 and TD4 on the remainder of the parallel system. The unfaulted subsystems continue to operate in parallel. However, TD3 and TD4 of the faulted subsystem continue to see the overcurrent condition. The signal from TD4 to trip the TBC may be provided but will have no affect on system operation since the TBC has already been tripped by TD5. A logical "PHI" or "don't care" condition is thus generated. The inverter overcurrent condition persists until TD3 has elapsed, tripping the load-bus contactor (column 15). The faulted load bus is thus isolated from the parallel system and the inverter which normally supplies the load bus. Since the inverter itself is not faulted but is prevented by the tripped LBC from supplying a load, the inverter control contactor (ICC) may be tripped or left closed, thus giving another "don't care" condition.

The truth table requirements for a Zone 1 overcurrent fault and for a load-division fault (columns 16 and 17) may be obtained directly from the earlier discussion "Control and Protection for Paralleled Static Inverters and Converters".

To provide a means of shutting down an unfaulted subsystem, the inverter control switch is used to provide a trip signal to trip the ICC, the LBC, and the TBC. These contactor trip signals must also prevent the load-division control and the load-division protection from operating. The phase-locking signal to the H bus is also removed. Column 18 of the truth table shows this action.

To implement the C/P circuits from the truth table, the logic statements governing each controlled or dependent variable are written from the columns of the truth table. For example, note that the load bus contactor close coil is activated from the logic condition of column 6. Reading vertically, LBC-Close must have the following conditions: MOS must be in the AUTO position; no abnormal voltage must exist; no abnormal frequency must exist; and no trip signals to the LBC must exist. This may be written symbolically as:

$$T2 = \text{LBC-CLOSE} = A \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{L} \qquad (1)$$

Equation (1) says: close the Load Bus Contactor only when (A) and (NOT D) and (NOT E) and (NOT F) and (NOT G) and (NOT L) are present.

Using reduction formulas, equation (1) can be rewritten as:

$$T2 = \text{LBC-CLOSE} = A \cdot \overline{(D+E+F+G)} \cdot \overline{L} \qquad (2)$$

Because the LBC-Close signal is required to activate other portions of the C/P circuits, a memory is required to ensure that this signal is available until the LBC is tripped even though the initiating signal disappears as, for example, during an undervoltage condition. Because the memory must be reset when the LBC is tripped, signal L is used to reset or remove the LBC-Close signal. A memory can be formed from a flip-flop or bi-stable latching circuit. LBC-Close memory can be generated by the statement:

$$T2 = \text{LBC-CLOSE (memory)} = A \cdot [\overline{(D+E+F+G)} + T2] \cdot \overline{L} \qquad (3)$$

This statement implies that once initiated, T2 can exist even though the NOR function, NOT $\overline{(D+E+F+G)}$, is not satisfied. Equation (3) can be further modified to become:

$$T2 = \overline{\overline{[\overline{(D+E+F+G)} + T2]} + \overline{L}} \qquad (4)$$

This statement is shown in the logic diagram (figure 4). Signal A, MOS-AUTO is not shown in equation (4) or on the logic diagram since this represents dc power to the C/P circuits. If signal A were not available, none of the C/P functions would operate. Therefore, A is understood to be present for all conditions shown in figure 4.

One more example will be given to show how the truth table is implemented. The dependent variable, TBC-TRIP may be satisfied by four different combinations of independent variables. This is shown in columns 13, 14, 17, and 18 of table II. The four conditions are OR conditions, i.e., any one or a combination of the four columns can trip the TBC. The equation for TBC-TRIP is then:

$$T6 = \text{TBC-TRIP} = \{[I \cdot K \cdot O \cdot P \cdot A] + [A \cdot U \cdot V] + [A \cdot R \cdot S]\} \cdot Z + A \cdot C \qquad (5)$$

Because time delays require sustained signals to cause them to time out, signals P, U, and S may be redefined:

$U \cdot V$ to U_V; read as Signal U after time delay V
$R \cdot S$ to R_S; read as Signal R after time delay S
$I \cdot K \cdot O \cdot P$ to $(I \cdot K \cdot O)_P$

Leaving Signal A out as before and providing a latching (M) and resetting (Z) function, equation (5) becomes:

$$T6 = \text{TBC-TRIP} = \overline{(I \cdot K \cdot O)_P + U_V + R_S + M + Z + C} \qquad (6)$$

Signal C is not made part of the memory circuit because it is derived from a manual switch, ICS. The reset signal, Z, is shown dotted in figure 4 because Z is derived by removing the dc power by switching MOS to the OFF or MANual position. This approach to resetting the memory circuit is explained in more detail in a later section "Logic Functions".

The implementation of column 19 is shown in figure 5. Normally, tuning-fork number 1 (TF1) provides all inverters with the 3200-Hz reference frequency. Tuning-fork number 2 (TF2) will take over whenever tuning-fork number 1 exhibits a failure. The failure of TF1 is determined by the frequency-reference protection circuit (FRP). The failure signal is stored in the flip-flop memory whose output simultaneously removes TF1 from the 3200-Hz bus and applies the output of TF2 to the 3200-Hz bus.

The tuning-fork oscillators are assumed to fail in one of two modes: either a very low frequency (1800 Hz or less) or the

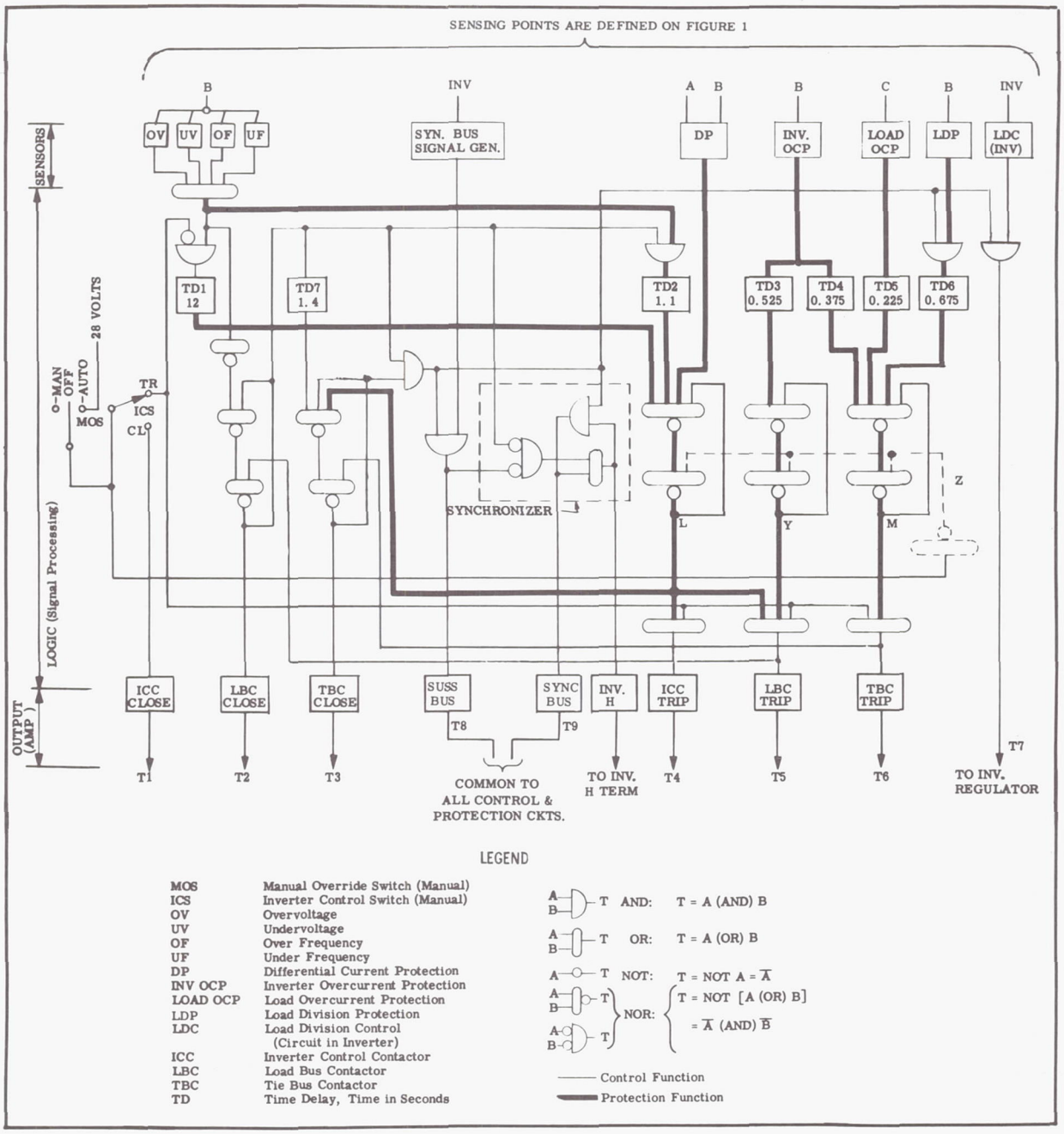


Figure 4. - Inverter Automatic Control and Protection

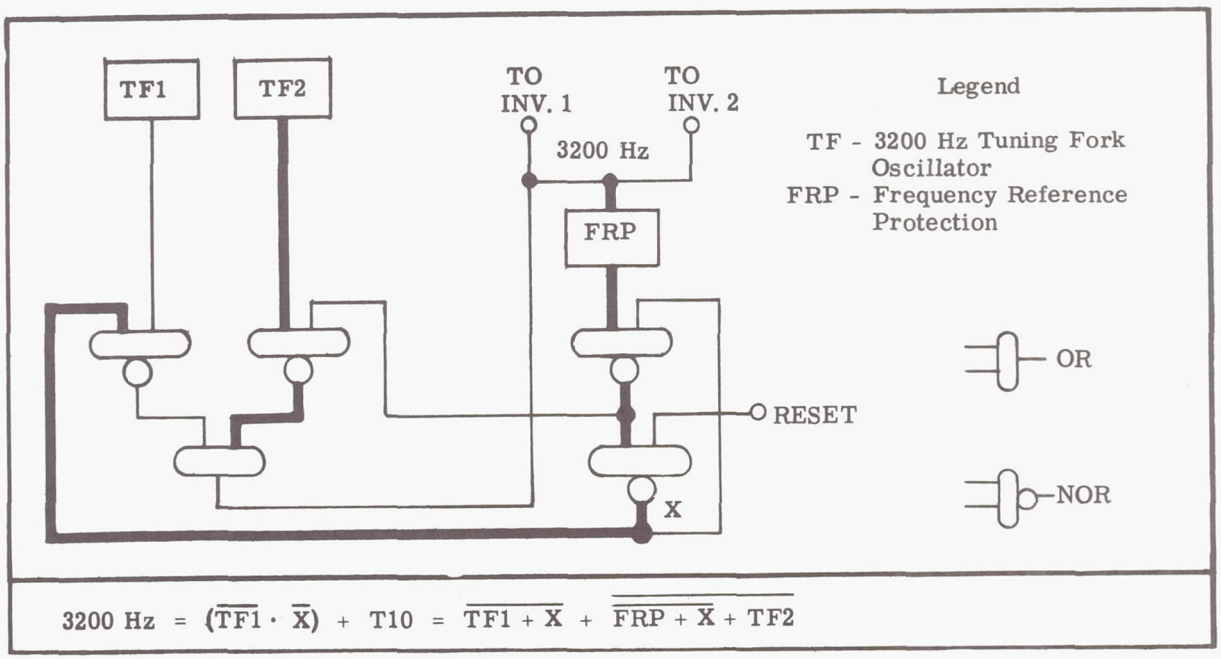


Figure 5. - Frequency Reference Protection

output becoming a constant amplitude dc signal. Since a tuning fork has a very narrow resonance curve, any failure in the driving mechanism will cause large variations in the output frequency. The sensing and transfer is so fast that the parallel system is not affected during this type fault. The reference oscillators may therefore operate independently of the parallel system. Moreover, the number of references need not equal the number of subsystems.

Table III lists the logic equations generated from table II. These equations were used to generate the logic diagrams of figures 4 and 5. The design of the sensing and signal processing (logic) circuits is described in the next section.

INVERTER CONTROL AND PROTECTION CIRCUIT DESIGN

This section provides an operational description of how each sensing, logic, and output function operates, the need for each type of circuit having been previously established. Figure 6 is a schematic diagram of the complete inverter control and protection circuit.

Table III. - Logic Equations for Inverter Control and Protection

Column Number in Truth Table	Dependent Variable (a)	Final Equations (b) (See table 2 for symbol definitions)
1	T1	$A \cdot B$
2, 3, 4, 5, 9, 10, 11, 12 & 16	L *	$\overline{\overline{[(D+E+F+G)\cdot\bar{C}]_h + [(D+E+F+G)\cdot I]_n + Q + Z}}$
13, 14 & 17	M *	$\overline{\overline{U_V + R_S + [I\cdot K\cdot O]_p + M + Z}}$
15	Y *	$U_W + Y + Z$
6	T2	$\overline{\overline{(D+E+F+G)} + T2 + T5}$
2, 3, 4, 5, 7, 9, 10, 12 & 16	T3	$\overline{\overline{L + I_j + T3} + T6}$
2, 3, 4, 5, 9, 10, 11, 12, 16 & 18	T4	$L + C$
2, 3, 4, 5, 9, 10, 11, 12, 15, 16 & 18	T5	$L + Y + C$
13, 14, 17 & 18	T6	$M + C$
8	T7	$I\cdot K\cdot$(LDC)
8	T8	$I\cdot K\cdot$(SUSS)
8	T9	$I\cdot K\cdot$(SYNC SIGNAL)
19	T10	$\overline{\overline{FRP + \bar{X} + TF2}}$ (pulse train from TF2)

a - Dependent variables with (*) are intermediate logic equations.

b - Lower case subscripts indicate that a time delay, corresponding to the CAP letter of table 2, must time-out before a fault signal is received.

Regulated DC Power Supply

All control and protection circuits are supplied power from an external dc power source when the Manual Override Switch is in the AUTO position. These circuits operate from 30 volts to as low as 20 volts at room temperature, thus allowing considerable variation in supplying voltage.

Time-delay circuits, however, require a constant voltage level because the capacitance charge time of a resistor-capacitor combination to charge to a predetermined voltage level is dependent on the magnitude of power supply voltage. Since power supply voltage can vary over a wide range, a voltage regulation circuit is needed.

Figure 7 shows the type of voltage regulator used in this design. Zener diode CR1 provides a constant dc voltage output. The current through the current-limiting resistor R1 varies with the applied voltage. The current through CR1 varies with the power demands on the circuit and the applied voltage. Therefore, the output voltage is held to the breakover voltage of the Zener diode. The tolerance for the breadboard system is ±5 percent.

Two regulated power supplies are used in each control and protection breadboard. They are shown in the schematic figure 6. The first (identified as 15VDC Reg. PS) provides a constant 15-volt output from pin P to the rest of the circuits. The regulator consists of current limiting resistor R54 and Zener diode CR34.

The second is located in the TFR transfer circuit. It consists of CR400 and R423. This power supply provides 18 volts for the system tuning-fork frequency reference and for the TFR transfer circuit.

Logic Functions

Five basic types of logic functions are used throughout the control and protection circuits of the inverter system: (1) the AND gate, (2) the OR gate, (3) the NOT or signal inversion, (4) time delays (sequential logic), and (5) locking circuits (memory logic). Each of these functions is described in detail below.

AND gate. - Figure 8a illustrates the common circuit and the symbol for AND gate. The three inputs (A), (B), and (C) must all be present for an output (T). Referring to the circuit, absence

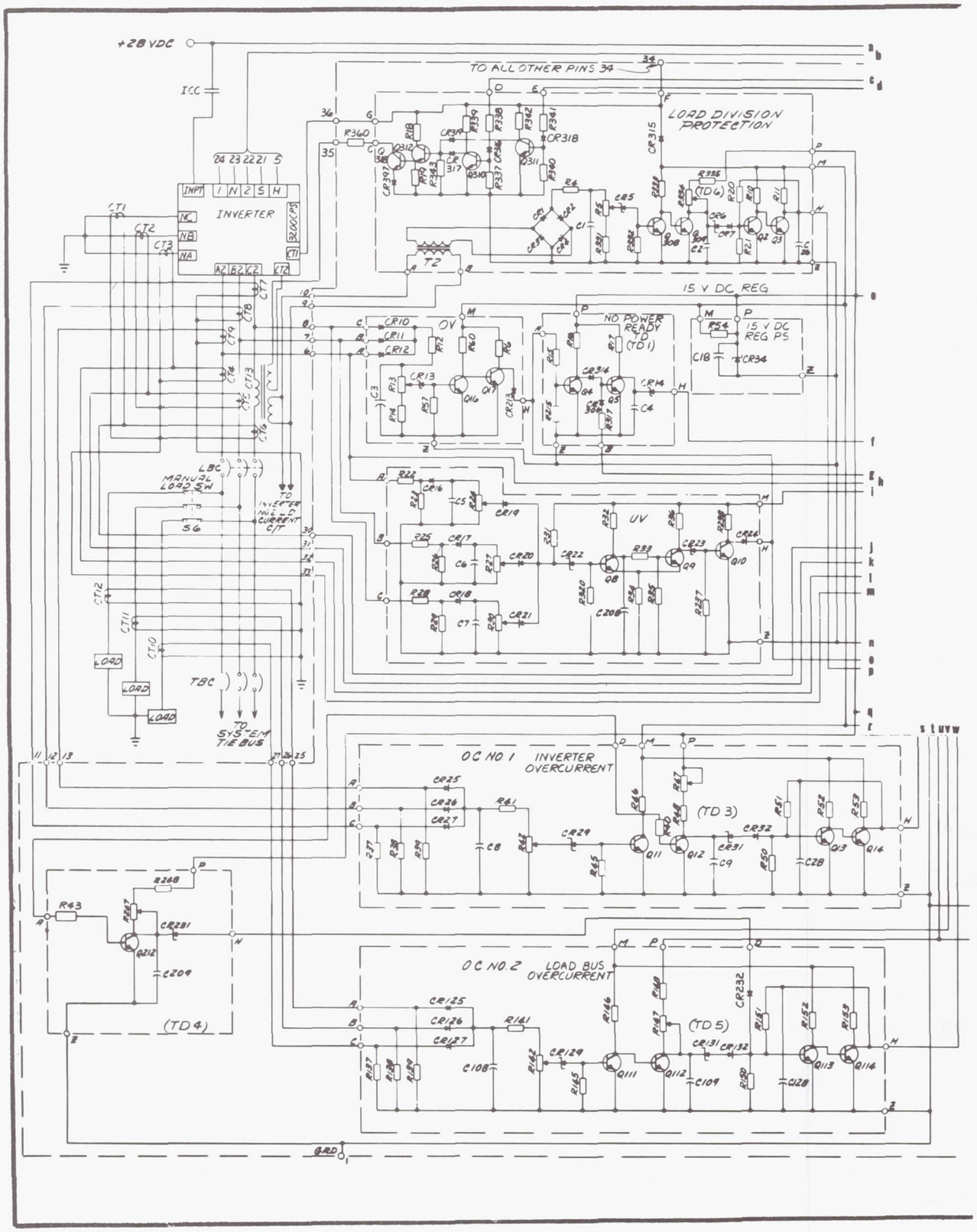


Figure 6. - Inverter Control and Protection Schematic

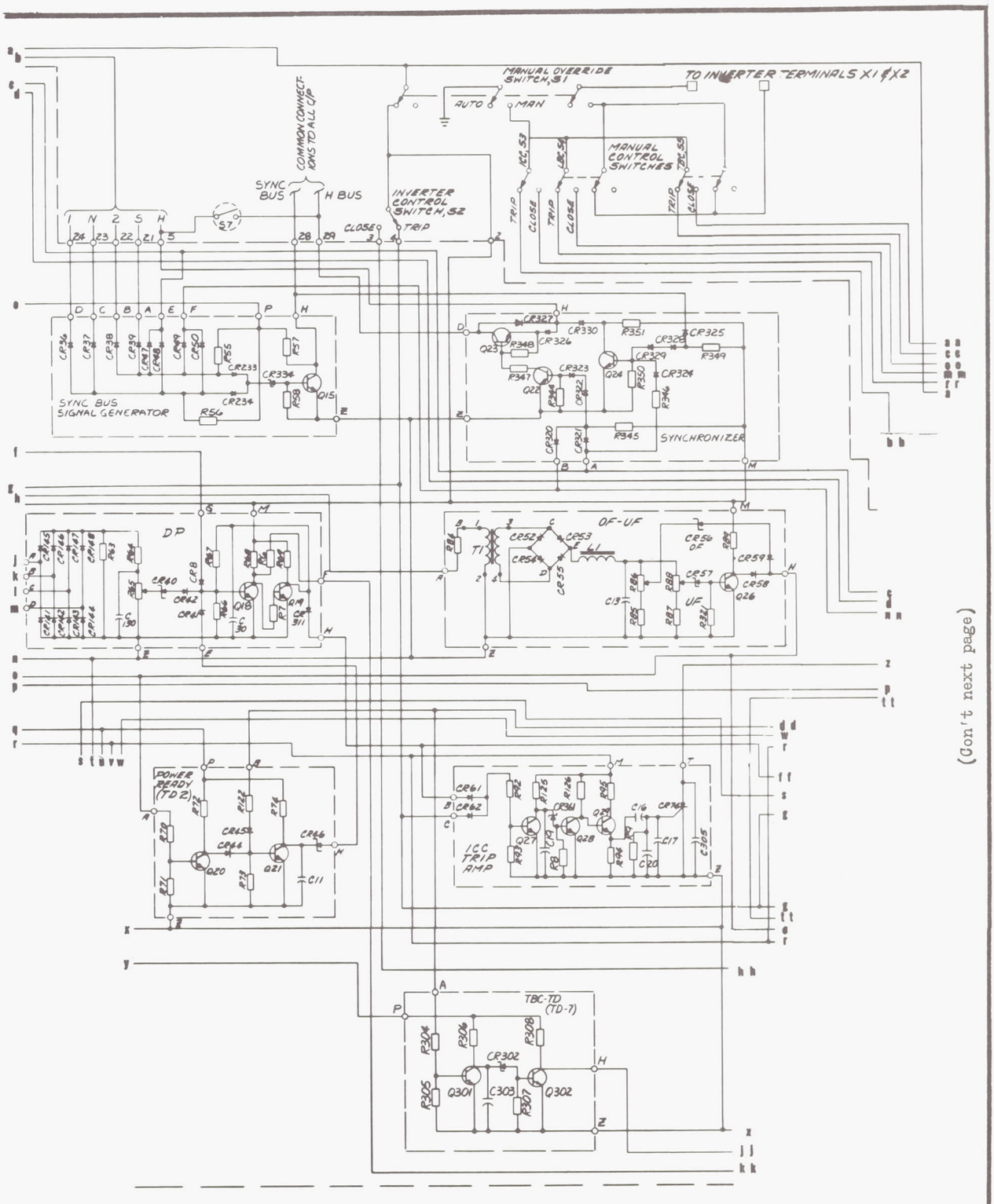


Figure 6. - Continued

(Con't from preceding page)

LEGEND
ICC - INVERTER CONTROL CONTACTOR
LBC - LOAD BUS CONTACTOR
TBC - TIE BUS CONTACTOR
OV - OVERVOLTAGE
UV - UNDERVOLTAGE
OF - OVERFREQUENCY
UF - UNDERFREQUENCY
DP - DIFFERENTIAL PROTECTION
CT - CURRENT TRANSFORMER
OC - OVERCURRENT
TD - TIME DELAY

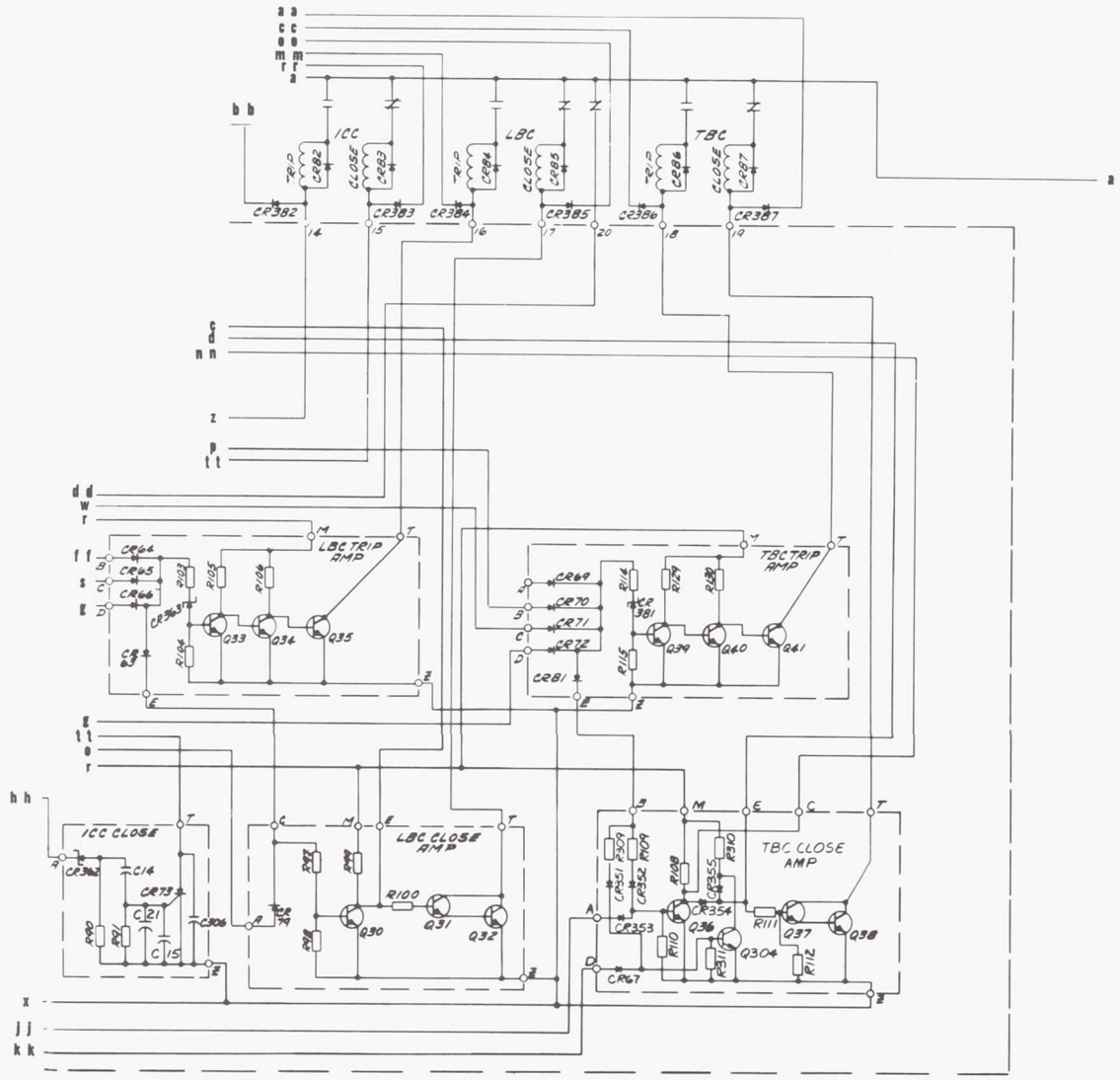
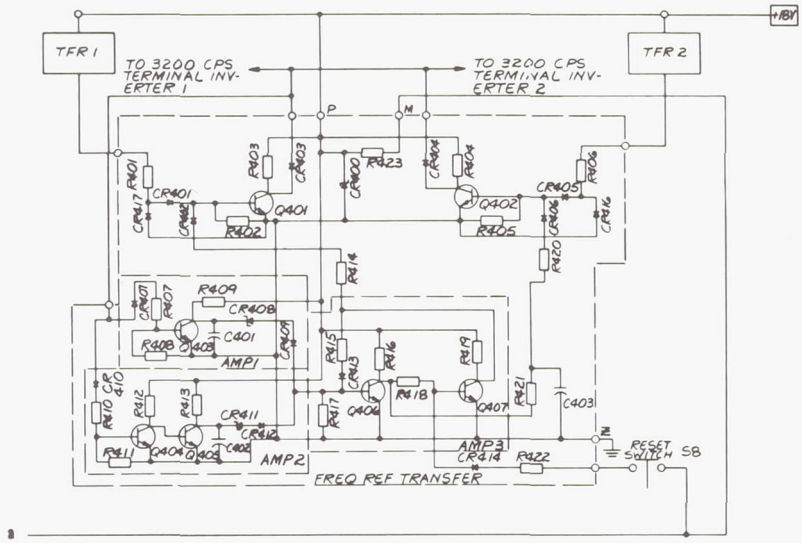
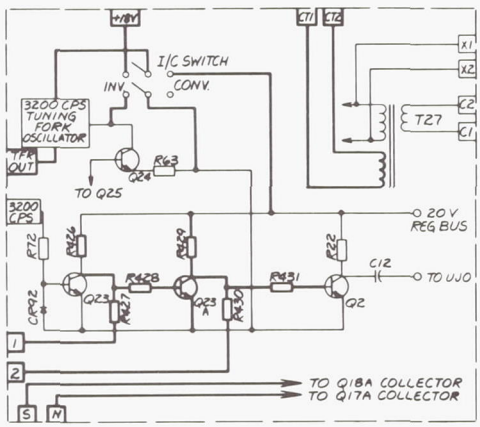


Figure 6. - Continued





MODIFICATIONS TO INVERTER
(ADDITIONS ARE IN HEAVY LINES)

Figure 6. - Continued

of either A, B, or C means that the respective input at the terminal is shunted through a transistor (not shown) to ground. This reduces the voltage level at the bottom end of R1, which is necessary to produce an output at T.

Diodes CR1, CR2, and CR3 isolate each input. Diodes CR4 and CR5 provide a threshold to assure no output at T when one of the inputs to CR1, CR2, or CR3 is zero (grounded).

OR gate. - The common circuit and the symbol for the OR gate is illustrated in figure 8b. Either input (A), (B) or (C) or any combination of the three will provide an output, (T). In the circuit, diodes CR6, CR7, and CR8 isolate each input.

NOT, or signal inversion. - The circuit and symbol for the NOT signal is shown in figure 8c. The symbol indicates that a positive input at A produces a zero output at T, and a zero input at A produces a positive output at T. The signal inversion is accomplished by passing the signal through a single-stage amplifier as shown in the circuit. A positive input through point A to the base of Q1 turns it on and shunts the collector voltage to ground. This eliminates the output at T. A zero signal into the base of Q1 turns it off and feeds a signal to point T from B+ through R2. The NOT circuit may be used in conjunction with the AND gate or OR gate to provide an NAND or NOR function.

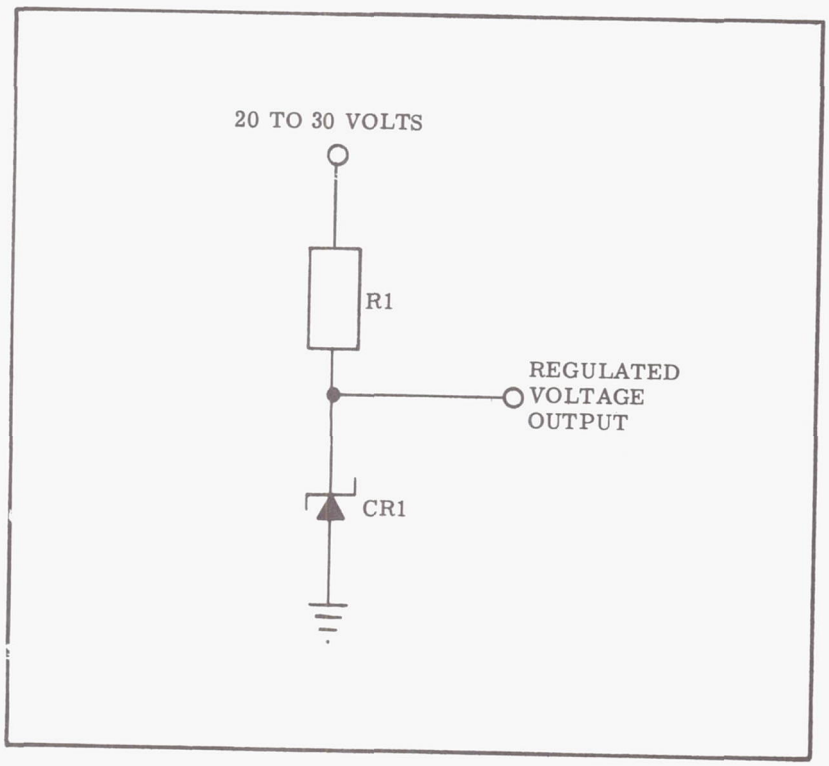


Figure 7. - A Regulated DC Power Supply

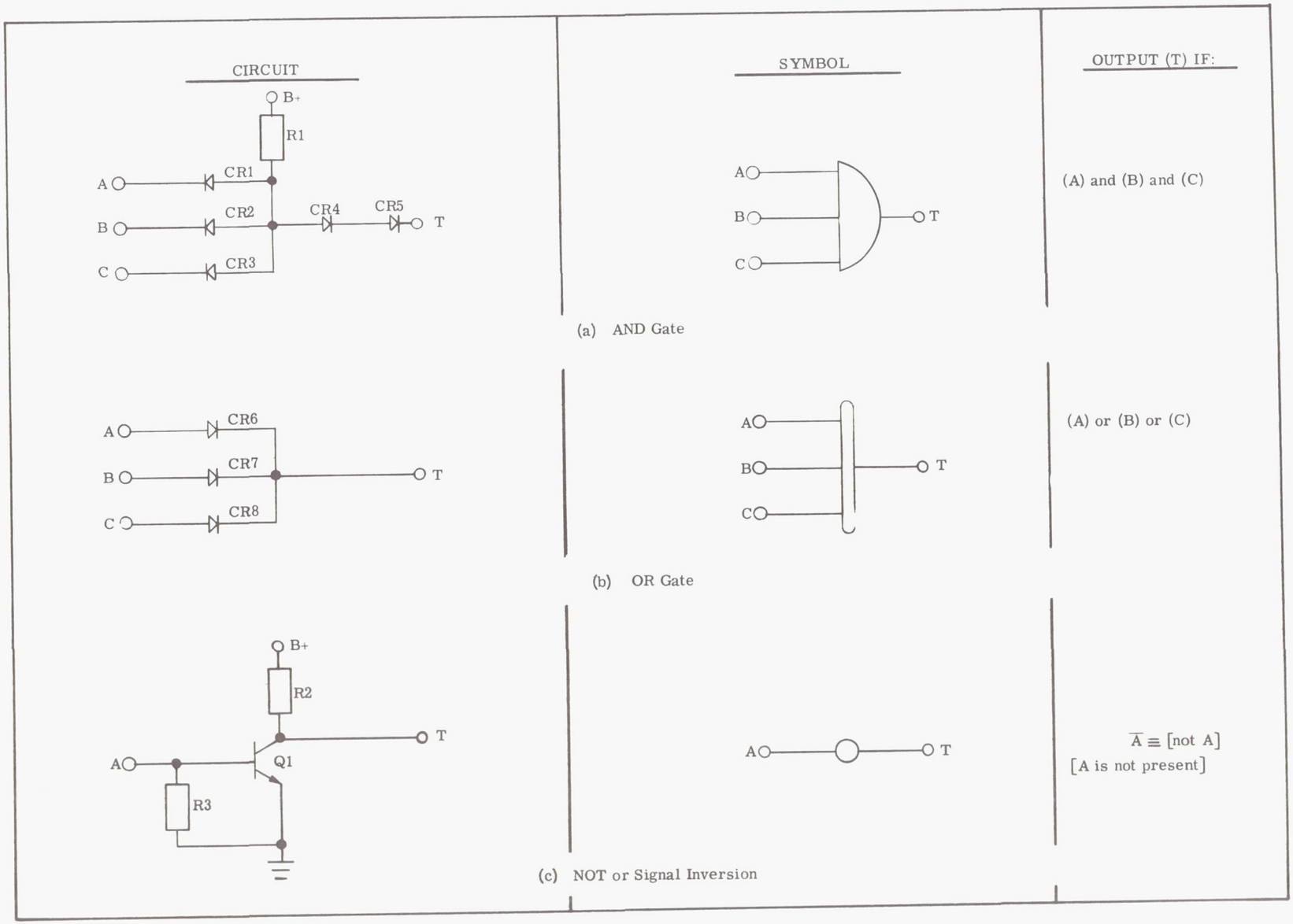


Figure 8. - Logic Functions

Time delays - sequential logic. - Time delays required to operate with system logic are provided by using resistor-capacitor (R-C) circuits (figure 9a). A positive voltage at point A applied to the base of transistor Q1 turns it on. This produces a low collector-to-emitter impedance and shunts the current through R1 to ground. The voltage across C1 is thus maintained at the saturation voltage of Q1 (about 0.3 volt). When Q1 is turned off, the high collector-to-emitter impedance across Q1 causes the current through R1 to be transferred to capacitor C1. The voltage across C1 will increase exponentially and, because a regulated voltage source is used, will require a fixed amount of time to reach the conduction voltage of CR1. When the Zener diode conduction voltage is reached, the circuit provides an output voltage at T. This signal is used by the logic circuits to operate the automatic protection.

Locking circuit - memory logic. - Locking circuits maintain a continuous output once they are energized. A signal will thus be maintained even if the initiating signal is removed.

Figure 9b illustrates the type of locking circuit used. Q1 remains off until a positive signal A is applied to its base. With Q1 off, Q2 will be turned on by the voltage applied through R2 and CR1. The output T is thus zero. A signal A to the base of Q1 will turn Q1 on and Q2 off, since the anode of CR1 is at ground potential. Thus, T has a positive output. Locking action is provided by feed-back signal T to the base of Q1 through R1 and CR3. Once Q2 is turned off, a continuous positive signal is supplied to the base of Q1 to hold it on, keeping Q2 turned off. This condition will be maintained even after the signal to the input A has been removed. A continuous output at T, independent of the initiating signal, is thus provided to perform the required logic functions. The capacitor, C1, is a spike suppressor which shunts spurious signals to ground to assure that the locking circuit does not switch until it receives an input signal A.

Two types of reset are available to unlock the circuit. One is to remove and then reapply the supply voltage. Capacitor C1 ensures that Q1 is off and Q2 is on when the voltage is reapplied to the circuit. The other type is to provide a reset signal to the base of Q2 as shown in figure 9b. If this method of circuit reset is used, diodes CR1 and CR2 must be used to isolate the two inputs to Q2. The reset signal passes through CR2. CR1 prevents Q1 from shunting the reset signal to ground. R5 is used to provide a path-to-ground for Q2 leakage current when it is turned off.

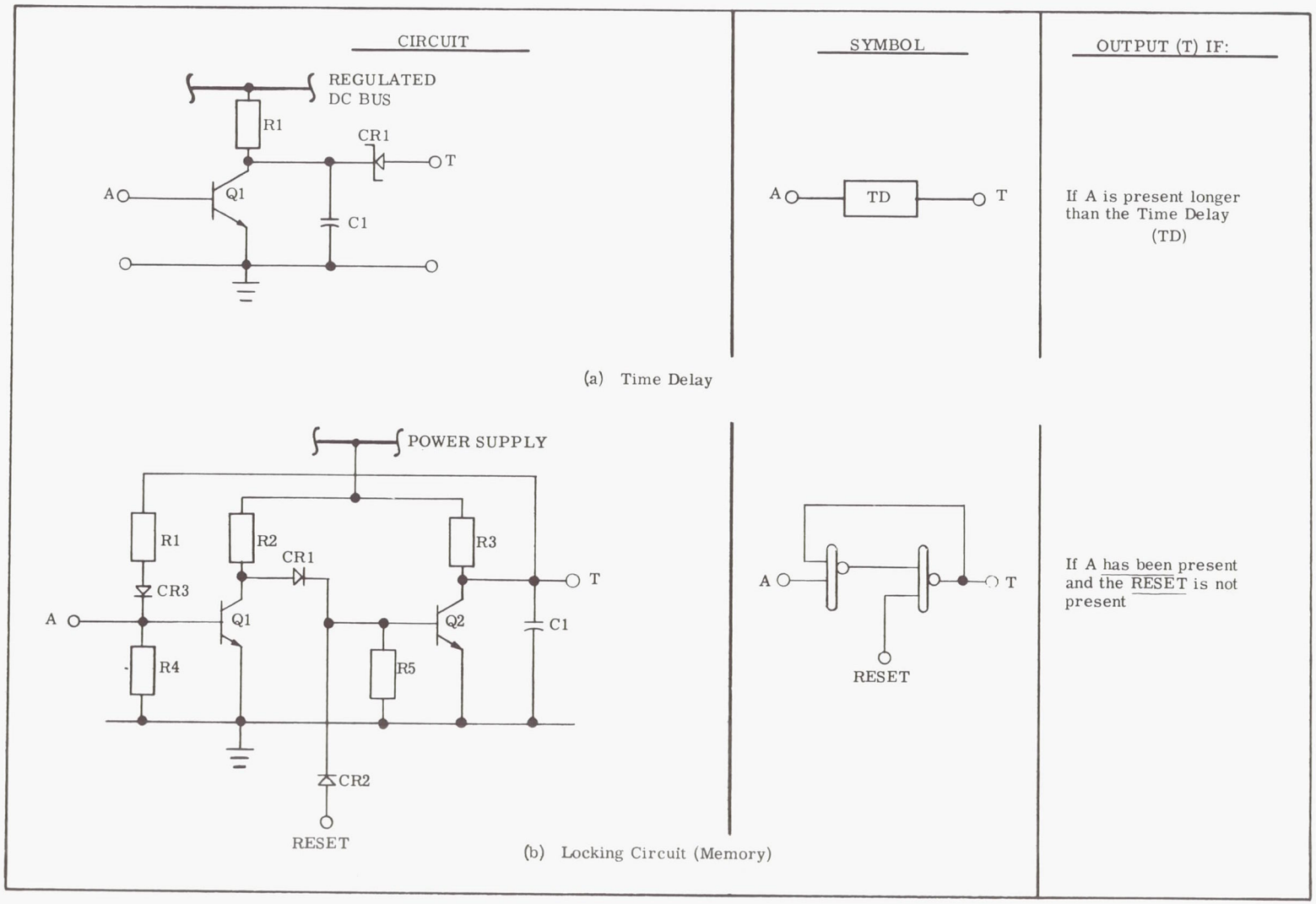


Figure 9. - Logic Functions

Inverter Control Contactor Close and Trip Amplifiers

The output stage of each amplifier is a silicon controlled switch requiring a gate pulse to turn it on. The function of the initial stages of these amplifiers is to shape the input signal into a short gate pulse. This minimizes the power consumed by the amplifier. It also prevents Inverter Control Contactor cycling since the amplifiers provide a pulse signal to the switch gate only at the start of an input signal. Thus, the input signal must be removed and reapplied for repeated operation. In addition, the trip amplifier is required to increase the low level of the signals from the protection circuits sufficiently to trip the inverter-control contactor (ICC).

ICC-close amplifier. - The ICC-close amplifier provides the signal to close the ICC. Closing the Inverter-Control Switch (ICS) turns CR73 on by providing a signal through C14 to the gate of CR73. The signal from the ICS is a constant voltage. However, the signal to the gate of CR73 is a pulse voltage. The pulse is provided because C14 blocks direct voltage but allows an initial pulse to pass through when a step voltage is applied. When CR73 is on, it provides a conduction path to ground for the close coil of the Inverter Control Contactor.

ICC-trip amplifier. - The ICC-trip amplifier controls the current through the trip coil of the ICC. The signals operating Q27 are shown in the logic diagram, figure 3. A signal to the base of Q27 turns it on. Then Q27 provides a path to ground for the signal at the base of Q28 turning it off. Q29 then receives a signal to its base through R126 turning it on to provide a path for a pulse signal to the gate of CR74 through C16. CR74 then switches to the conducting state and provides a path to ground for the current through the trip coil of the Inverter Control Contactor.

Control of Load-Bus and Tie-Bus Contactors

Control of the load-bus and tie-bus contactors for each subsystem is provided by static amplifiers during automatic operation. These amplifiers receive signals from the inverter control and protection circuits as shown in figure 3. The amplifiers increase the power level of the C/P signals to handle the contactor actuation current.

LBC-close amplifier. - The LBC-close amplifier controls the signal to the close coil of the LBC. The amplifier, shown in figure 6, receives its close signal at the collector of Q30 through R99 when the Inverter Control Switch is closed. This

transistor is kept turned on (until the proper time to close the LBC) by a positive signal to its base through R97 from either of the two logic signals shown in figure 3. When a power-ready condition exists and no system fault signals are present, Q31 receives a signal to its base through R99 and R100. Transistors Q31 and Q32 comprise a Darlington coupled amplifier which controls the current through the close coil of the LBC. When Q31 is on, it provides base drive to Q32 to keep Q32 turned on also. Q32 then supplies a current path to ground for the LBC close coil. This closes the contactor.

The connection to pin E provides a positive signal to the load-division protection circuit whenever the LBC is closed. This signal is used by the load-division protection circuit to control lockout of the load-division control and load-division protection current transformers as described later under "Load-Division Protection".

LBC-trip amplifier. - The LBC-trip amplifier controls the current through the trip coil of the LBC. The controlling signals are shown in figure 3. The circuit schematic is shown in figure 6. The diodes CR64, CR65, and CR66 comprise an OR gate. A signal to any of them energizes the amplifier and also sends a signal through CR63 to the LBC-close amplifier maintaining it inactive as long as the LBC-trip amplifier receives a signal. The signal passes through R103 and Zener diode CR363 to the base of Q33 turning it on, turning Q34 off and turning Q35 on. CR363 prevents spurious noise signals from energizing the amplifier. Turning Q35 on provides a path to ground for the trip coil of the load-bus contactor.

TBC-close amplifier. - The TBC-close amplifier controls the current through the close coil of the TBC. The controlling signals are shown in figure 3. The circuit schematic is shown in figure 6. Q36 and Q304 are used as a NOR circuit. If either Q36 or Q304 is turned off, a signal is fed through R111 to the base of Q37. This energizes the Darlington coupled amplifier, Q37 and Q38. Q38 turns on and provides a ground path for the close coil of the TBC. This closes the tie-bus contactor. The connection to pin E provides a signal to the load-division protection circuit whenever the TBC is closed. This signal is used to control lockout of the load-division control and load-division protection current transformers as described later under "Load-Division Protection".

TBC-trip amplifier. - The TBC-trip amplifier controls the current through the trip coil of the TBC. The controlling signals are shown in figure 3. The circuit schematic is shown in figure 6. The diodes CR70, CR71, and CR72 comprise an OR gate. A signal to any of them will energize the amplifier and also send a

signal through CR81 to the TBC-close amplifier maintaining it inactive as long as the TBC-trip amplifier receives a signal. The signal passes through R114 and CR381 to the base of Q39 turning it on, turning Q40 off and Q41 on.

CR381 prevents spurious noise signals from energizing the amplifier. Turning Q41 on provides a path to ground for the trip coil of the tie-bus contactor.

Overvoltage Sensing

The overvoltage protection circuit, identified as OV in the schematic diagram, figure 6, senses the average of the inverter bus voltage. Average-phase sensing was chosen over highest-phase sensing to be compatible with the average-sensing voltage regulator. The selected trip range for this circuit is 120 to 126 volts, rms, line-to-neutral.

The phases are sensed through CR10, CR11, and CR12 which halfwave rectifies the voltage. R12, R13, R14, and C3 make up a voltage divider and filter which produce a dc output proportional to the average magnitude of the ac bus voltage. R13 provides an adjustment to set the OV limits. The voltage developed from the arm of R13 to ground is applied to Zener diode CR13. When the conduction voltage of CR13 is exceeded, Q16 is turned on and Q17 is turned off. An overvoltage signal is provided through R16 and CR213 to the H-terminal of the OV circuit board. The H-terminal is connected to TD1, TD2, and the LBC-close amplifier.

Undervoltage Sensing

The undervoltage protection circuit, identified as UV in the schematic diagram, figure 6, senses the lowest phase of the inverter three-phase output. It provides a constant dc output when any phase of the inverter voltage remains below a set value. The value is adjustable for each phase and is set within the trip range of 102 to 108 volts rms. Although an average-phase-sensing, undervoltage protection circuit is simpler, the lowest-phase-sensing circuit provides a measure of open-phase protection.

Each phase is sensed through identical networks. For example, phase A, inverter output voltage is applied across voltage divider R22 and R23. The junction of these two resistors is connected to diode CR16 which rectifies the alternating voltage. Capacitor C5 filters the voltage to produce a positive direct voltage across potentiometer R24 proportional to the inverter output voltage on phase A. The potentiometer is adjusted so that the junction between R21 and R24 maintains sufficient voltage level to keep Zener diode CR22 conducting and transistor Q8 turned on so long as

the inverter output voltage is above the undervoltage limit. When Q8 is on, Q9 is off. As long as Q9 remains off, the voltage at Zener diode CR23 is sufficient to maintain Q10 in the conducting state. This, in turn, provides the current drive to keep Q10 on and prevents an output from the undervoltage circuit. The voltage at CR22 depends on the current through the divider network of R31 and the portion of R24 between the tap and ground as well as the current through R24 from the rectified bus voltage. Therefore, R24 is set so that a bus voltage below the undervoltage limit will bring the voltage at Zener diode CR22 below its conducting threshold and permit transistor Q8 to turn off. Turning off the current through Q8 increases the voltage at the base of transistor Q9 sice the current through the network R32, R33, and R35 increases. At the same time, it tends to reduce the voltage across R34 and bring the emitter of Q9 toward ground potential. This double effect quickly turns on transistor Q9. C208 is a spike suppressor to keep Q9 off until this double action takes place. When Q9 conducts, its collector voltage is below that which will support conduction through Zener diode CR23. Therefore, transistor Q10 will turn off. This provides a constant positive output through diode CR23 which indicates an undervoltage condition. The output will persist as long as the undervoltage condition exists. The output of this circuit supplies signals to TD1, TD2, and LBC-close amplifier.

Abnormal Frequency Sensing

The abnormal frequency sensing circuit, identified as OF-UF in figure 6, monitors the inverter output frequency. The output frequency is sensed by connecting saturable transformer T1 across one phase of the inverter. A bridge rectifier and an L-C filter are connected across the secondary of T1. The voltage developed across C13 is proportional to the volt-seconds absorbed by T1. The circuit is arranged so that T1 saturates very early during each half cycle of inverter output voltage, within 10 to 20 degrees. The secondary voltage of T1 is then a series of triangular pulses 10 to 20 degrees long which are applied to the L-C filter. Because the transformer saturates very early each half cycle, the volt-seconds applied to the filter is relatively insensitive to actual magnitude of phase voltage. For example, if T1 saturated at 15 degrees with normal voltage applied, the volt-second output would be nearly the same if the voltage were reduced to 10 to 20 percent of rated. Since the volt-seconds per cycle is relatively constant (independent of voltage level), the output of the frequency sensing circuit will be directly proportional to the number of pulses per second or the output frequency. Reference 3 includes a detail description of this sensing circuit.

Calibration of the OF-UF sensing is determined by the voltage dividers R85 and R86 for OF, and R87 and R88 for UF. The voltage dividers are connected across the filter capacitor C13. Potentiometer R86 is adjusted so that the voltage from arm-to-ground will cause Zener diode CR56 to conduct whenever the frequency is in the 404 to 410-Hz range, thus providing a signal to pin H through CR59.

The underfrequency trip point is set by adjusting potentiometer R88 to cause Zener diode CR57 to conduct whenever the output frequency is above the trip range of 390 to 396 Hz. CR57 then turns Q26 on whenever the frequency is above the trip range. The output of the UF circuit is zero since the anode of CR58 is grounded. Should an underfrequency condition exist, Q26 is turned off because the voltage from the arm-to-ground of R88 is below the zener conduction voltage. The UF signal is then applied to pin H through R89 and CR58.

Pin H, which receives a signal from either the OF or the UF sensing circuit, is connected to TD1, TD2, and the LBC-close amplifier.

Frequency Reference Protection

The frequency reference protection provided causes immediate switching to a second tuning-fork frequency reference if the first one fails during either automatic or manual operation. The circuit which provides this function is the system FREQ REF TRANSFER circuit which is located separate from the control and protection breadboards, figure 6. At startup both tuning-fork references (TFR) are energized. TFR1 is the unit normally used as the system master driver while TFR2 is the standby unit. The frequency reference transfer circuit continuously monitors the output of the tuning-fork frequency reference. The square wave output of TFR1 is supplied through R401 and CR401 to the base of Q401. Q401 amplifies this signal. Its output is then applied to the 3200-Hz line through CR403. The 3200-Hz line is used to drive the unijunction oscillators in each inverter, thus maintaining all inverters at the same frequency.

The signal from the 3200-Hz line is also fed to the base of Q403 through CR407 and R407. This signal is a 3200 cycle-per-second square wave. This square wave turns Q403 alternately on and off for equal time periods. As long as the 3200-Hz square wave is applied to the base of Q403, capacitor C401 is alternately charged and discharged. The voltage developed across C401 is thus prevented from reaching the breakdown voltage of Zener diode CR408. Thus, this circuit, identified as AMP1, provides no

output during normal operation. For the same reason, the circuit identified as AMP2 provides no output during normal operation.

The outputs of these two amplifiers are fed to the input of a third amplifier identified as AMP3. AMP3 is a self-locking flip-flop which provides a continuous output once it has been energized. This amplifier remains in the unlocked state until it receives a signal from either AMP1 or AMP2. Under normal conditions, Q406 remains off and provides a signal through R418, CR414, R421, R420, and CR6 to the base of Q402. This keeps Q402 turned on and isolates the output of TFR2 from the 3200-Hz line by diode CR404, thus preserving the signal from TFR1 as a system reference during normal operation.

The TFR unit has two modes of failure: (1) zero voltage or low frequency output, or (2) a constant positive output. AMP1 senses for the first mode of failure and AMP2 senses for the second.

Zero input to the two amplifiers caused by a mode (1) failure turns Q403 off allowing C401 to charge through R409. When the conduction voltage of Zener diode CR408 is reached, the amplifier provides an output to AMP3 through CR409.

Under this condition Q404 of AMP2 is also off since it receives no base input. Q405 is then held on by current drive through R412. The voltage across C402 remains at the level across Q405. Thus, the conduction voltage of Zener diode CR411 is not reached, and the circuit provides no output. The output from AMP1 due to this mode of failure energizes AMP3. Energizing AMP3 causes the amplifier to change state allowing Q406 to turn on and Q407 to turn off. Turning on Q406 removes the signal normally fed to the base of Q402 through R421, R420, and CR406 and allows Q402 to function as an amplifier. Thus, the output of TFR2 is amplified and fed to the 3200-Hz line through CR404.

At the same time the output from TFR1 is isolated from the 3200-Hz line because Q407 turns off and supplies a signal to the base of Q401 through R414 and CR402. This keeps Q401 on, removing its output from the 3200-Hz line.

In case of a mode (2) failure, a continuous positive signal is fed to the inputs of AMP1 and AMP2. This signal keeps Q403 on. C401 cannot charge up to the conduction voltage of CR408. Thus, AMP1 provides no output. The input signal also keeps Q404 on. This in turn switches Q405 off and C2 charges through R13 until the conduction voltage of Zener diode CR411 is reached. AMP2 then provides an output through CR412 to energize AMP3. This amplifier then switches states and provides the proper outputs to isolate TFR1 from and connect TFR2 to the 3200-Hz line as

with the mode (1) failure. The reset switch, S8, applies 28 volts through R422 and CR415 to the base of Q407. This turns on Q7. If an input to AMP3 is no longer present because normal output from TFR1 has been restored, Q6 will turn off and the amplifier will revert to its original state. In this case the circuit will switch back to TFR1 as the reference and isolate TFR2.

Differential-Current Sensing

Differential-current protection is provided by six current transformers and the circuit identified as DP in figure 6. The current transformer and DP portion of figure 6 is reproduced in figure 10. The DP circuit senses any fault currents between the

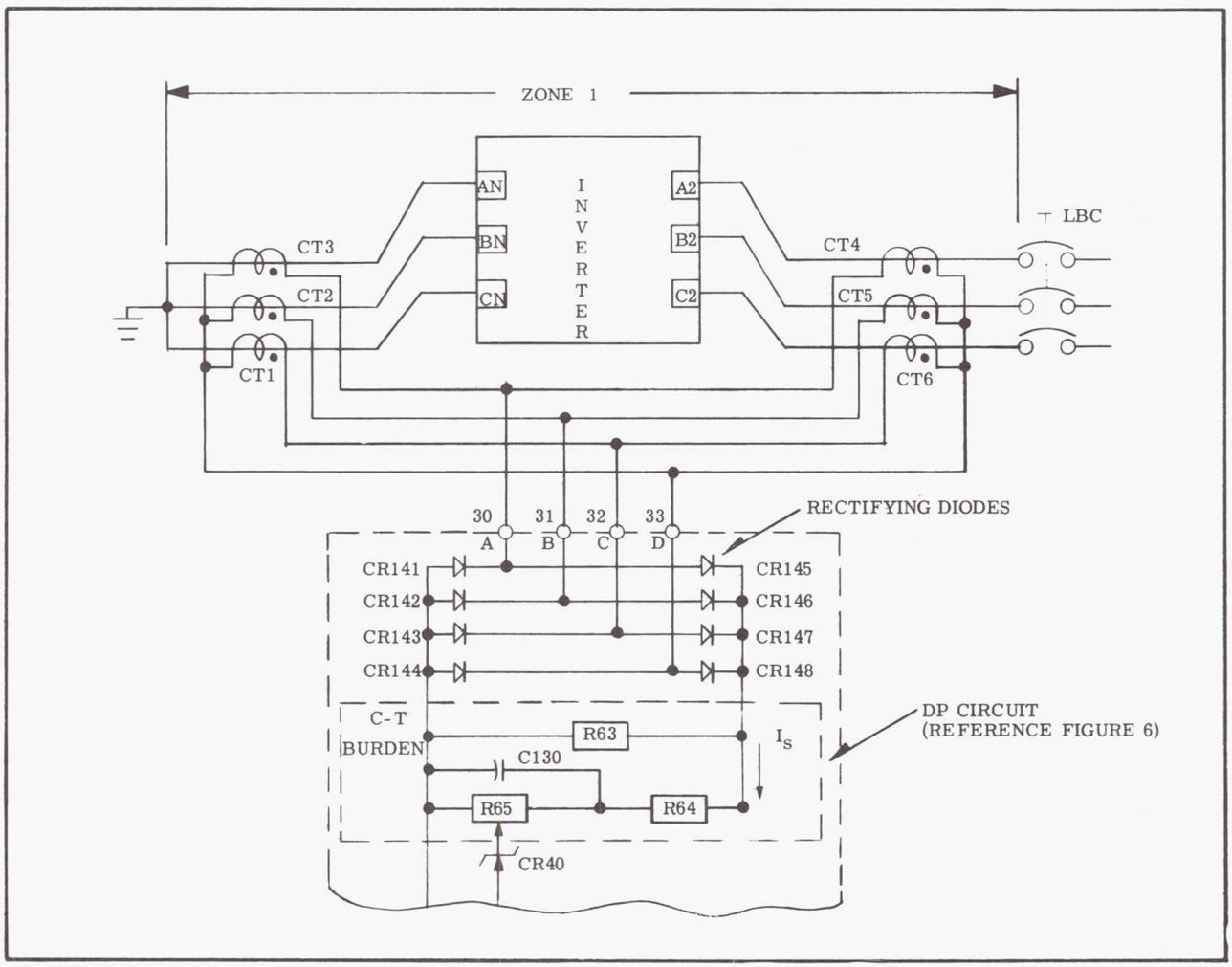


Figure 10. - Differential-Protection, Sensing-Circuit Connection

terminals of the inverter and the load-bus contactor by sensing the current in each phase at two locations, as shown in figure 10. The secondaries of each pair of transformers are connected in series; that is, the connection provides a low impedance path for circulating currents. Since a current transformer operating in its linear range is a current-source type of power supply, the secondary current cannot be changed by an external source. Using this fact, a fault or difference current can be sensed by monitoring the voltage developed across the burden of the C-T pair. Figure 11 shows one phase of the DP sensing circuit. The dots on the C-T secondaries show the relative current polarities. If the C-T's of figure 11 are identical, the exciting currents are neglected, and there is no fault current ($I_f = 0$), the secondary currents are equal and in phase. Therefore, the voltage drop across the C-T is zero and no current flows in the burden resistor R. If I_f is not zero, I_{s2} is not equal to I_{s1}, and excess circulating current is forced to flow through the burden resistor.

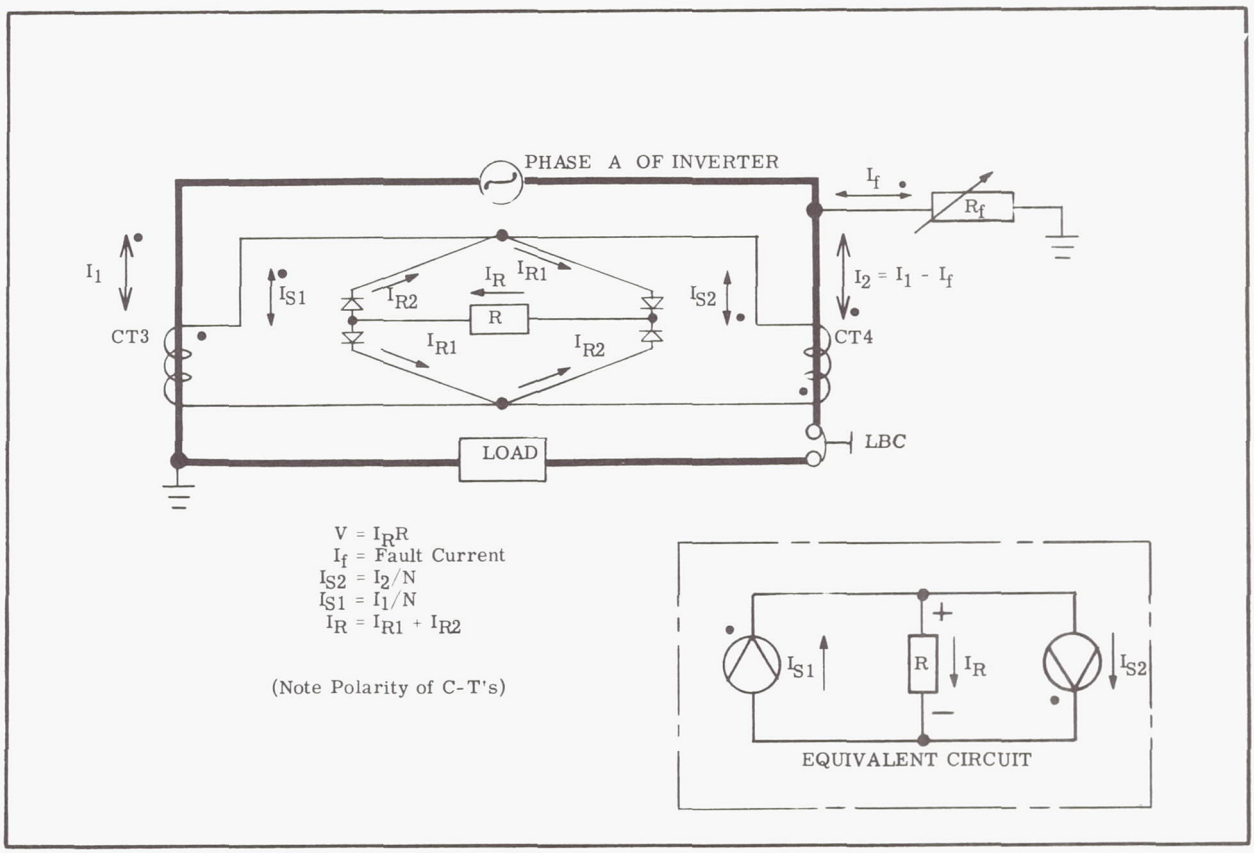


Figure 11. - Simplified Differential-Protection, Current-Transformer Loop

Summing the currents in the equivalent circuit, figure 11,

$$I_{s1} = I_R + I_{s2} = I_R + (I_1 - I_f)/N = I_R + I_{s1} - (I_f/N).$$

The current in the resistor is therefore directly proportional to the fault current I_f. Hence, the voltage across the resistor is

$$V = I_R R = I_f R/N.$$

Referring to figure 10, a line-to-neutral fault will produce a difference current in one phase, thus involving only one C-T loop. A line-to-line fault will produce a current differential in two phases, thus involving two loops. Therefore, either a line-to-neutral or a line-to-line fault is sensed.

The bridge rectifier shown consists of eight diodes (CR141 through CR148). The difference current will flow through a combination of these diodes. Therefore, the bridge is a single-phase bridge, for any combination of line-to-ground or line-to-line faults or a three-phase bridge for a three-phase fault. Tracing the current path of I_s through the diodes in the forward direction shows that the difference current developed in one or a combination of C-T loops must flow through the burden (R63 in parallel with R64 and R65). The C-T burden establishes a voltage level compatible with the rest of the circuit. Capacitor C130 filters the output of the bridge. Potentiometer R65 provides a means of calibrating the DP sensing circuit.

R65 is adjusted so that Zener diode CR40 conducts at the selected trip point. The trip range for the differential protection is 0.87 to 1.3 differential amperes in primary current in any phase. The signal from CR40 passes through CR42 to the base of Q18. Referring to figure 6, a signal can also be fed to Q18 through CR41, CR8, or R67. Q18 and Q19 act as a memory circuit to provide a continuous output until reset by removing and reapplying the supply voltage. The output of the memory circuit is fed to the ICC-trip amplifier, the LBC-trip amplifier and the TBC-close amplifier.

Overcurrent Sensing

How overcurrent sensing is used to provide system overcurrent protection was discussed in "Inverter Control and Protection". System overcurrent sensing is provided by two circuits

in each subsystem protection breadboard. These circuits are identified as OC No. 1 and OC No. 2 in the schematic diagram, figure 6. The method of current sensing is described below.

Inverter overcurrent. - OC No. 1 (INV OC) monitors the current in each phase at the output terminals of the inverter by means of current transformers CT7, CT8, and CT9. R37, R38, and R39 are burden resistors which are connected across the current transformer secondary windings. These resistors provide a secondary voltage level compatible with the rest of the C/P circuits and also ensure that the transformers are not driven into saturation over the range of current. The voltages developed across the three burden resistors are half-wave rectified by CR25, CR26 and CR27 and filtered by C8 to provide a voltage proportional to the inverter output current. This output is applied across voltage divider R41 and R42. R42 provides an adjustment for calibration of OC No. 1. The trip range for this circuit is 2.5 to 2.73 amperes (1.15 to 1.25 per unit).

An overcurrent condition increases the voltage across R42 to cause Zener diode CR29 to conduct. The current through CR29 turns Q11 on, shunting the base drive of transistors Q12 and Q212 to ground and starting time delays TD3 and TD4.

Load-bus overcurrent. - OC No. 2 (Load OC) monitors the current in each phase of the load bus by means of current transformers CT10, CT11, and CT12. R137, R138, and R139 provide a burden across the secondary windings of the current transformers. These resistors provide a voltage level compatible with the rest of the circuit and also ensure that the transformers are not driven into saturation over the range of current. The voltage developed across the three burden resistors is half-wave rectified by CR125, CR126, and CR127 and filtered by C108 to provide an output proportional to the load-bus input current. This output is applied across voltage divider R141 and R142. R142 provides an adjustment for calibration of OC No. 2. The trip range for this circuit is 2.5 to 2.73 amperes (1.15 to 1.25 per unit).

An overcurrent condition increases the voltage across R142 to cause Zener diode CR129 to conduct. The current through CR129 turns Q111 on, shunting the base drive of Q112 to ground. This starts time delay TD5.

Load-Division Protection

Operational description of current transformer lockout circuit. - When a subsystem is not paralleled to the system tie bus, the load-division control and protection circuits must be

disabled. Disabling the control circuit prevents control signals from acting on the voltage regulator circuits. Disabling the protection circuit prevents false tripping of the TBC.

The method chosen for this inverter system is to effectively short circuit the current transformers by saturating their cores. This is accomplished by an auxiliary winding on the LDP current transformer CT13. The auxiliary winding of the LDC current transformer, located within the inverter, is connected to the C/P circuits by terminals CT1 and CT2. The auxiliary windings of the two transformers are connected in series. The current through the auxiliary windings is controlled by transistor Q318 in the load-division protection circuit of figure 6. The circuit consists of a 28-volt source (pin 36), through auxiliary winding of LDC and LDP C-T's, current limiting resistor R360, Q318, and CR397 to ground. Sufficient current flows to saturate the cores under all load currents of an isolated subsystem. The secondary impedance of the saturated C-T's is reduced to 2 or 3 ohms resistive.

Transistor Q318 is controlled by signals from the LBC-close amplifier and the TBC-close amplifier. The signal from the LBC-close amplifier, collector of Q30, is fed through R338 and CR316 to the base of Q310. This signal keeps Q310 turned on when the LBC is closed. Similarly, the signal from Q36, in the TBC-close amplifier, is fed through R341 and CR318 to the base of Q311 turning Q311 on when the TBC is closed. When both Q310 and Q311 are on, both Q312 and Q318 remain off, thereby distrupting the current through the dc bias windings on the subsystem current transformers in the load-division-control and load-division-protection loops. The current transformer cores are thus unsaturated and function normally within the system loops.

If either the load-bus or tie-bus contactor open, the respective contactor close amplifier will no longer supply a signal to the lockout circuit. Either Q310 or Q311 will be turned off and will supply a signal to turn on the current coupled amplifier Q312 and Q318. Under this condition Q318 provides a path for the bias or C-T saturating current.

Operational description of load-division sensing circuit. - Load-division protection (LDP) senses the unbalance current developed when the load-division control circuits fail to maintain the current balance between inverters within the specified tolerance. The allowable current unbalance for this system is ten percent of rated current. The protection circuit must provide a signal to isolate the subsystem whenever the current unbalance exceeds this limit. The LDP is designed to trip for current unbalances between ten and twenty percent of rated current. The current sensing arrangement is shown in figure 12. Note that the

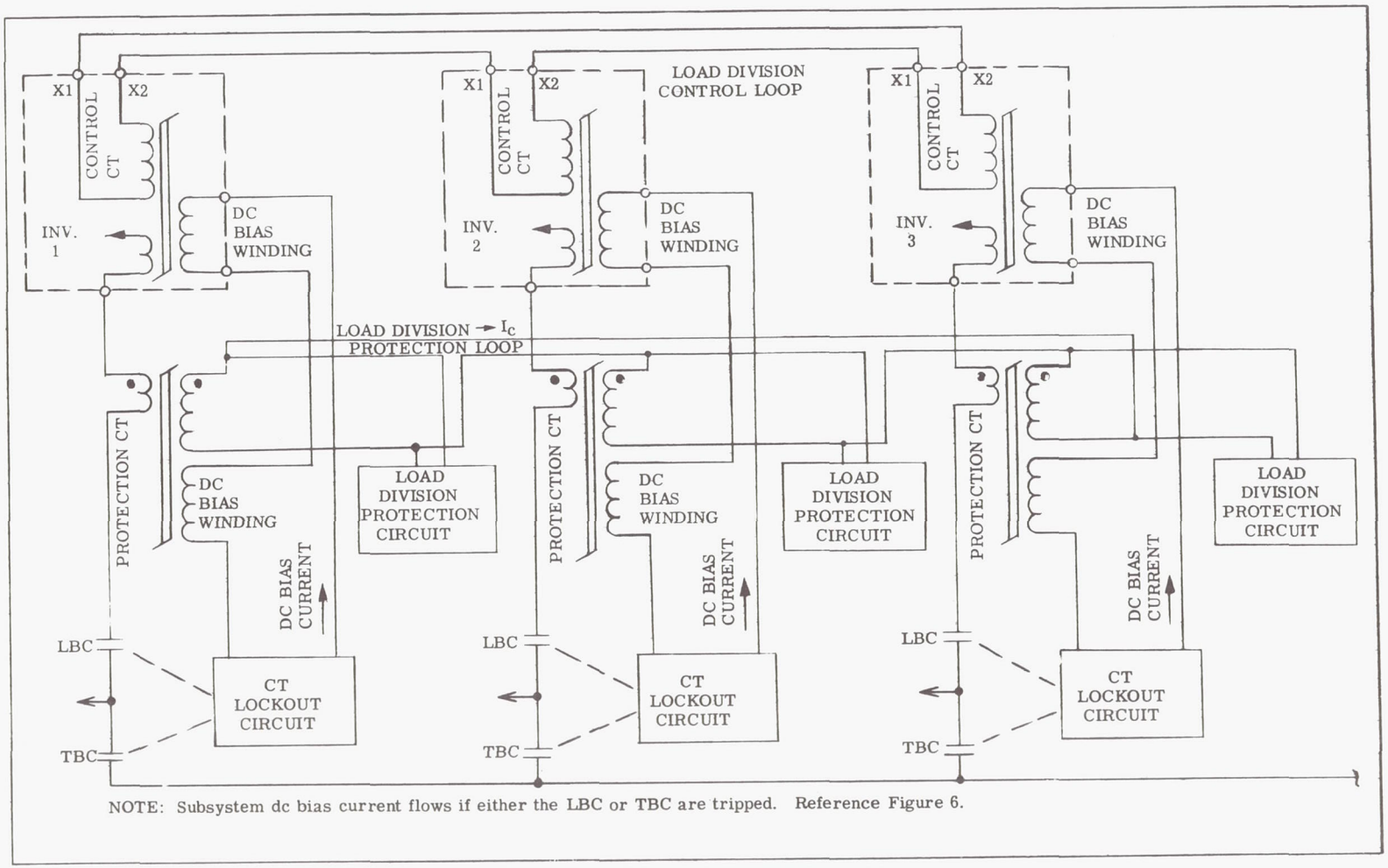


Figure 12. - Load Division Control and Protection Current Transformer Connections

current transformer secondaries are connected in series. Hence, the current transformers are connected much like the Zone 1 differential current protection circuit except that the number of current transformers connected in series is equal to the number of paralleled subsystems. Like the DP C-T's, any unbalance current is forced to flow in the C-T burdens. Transformer T2 of figure 6 provides the burden for the C-T's. Transformer T2 provides three functions: (a) a burden for the current transformer, (b) circuit isolation for the LDP sensing circuit, and (c) a means of stepping up the C-T secondary voltage.

The secondary voltage of T2 is rectified by the full-wave bridge rectifiers (CR1, CR2, CR3, and CR4) whose output is applied across R4, R5, and R331. Capacitor C1 filters the rectified voltage. Potentiometer R5 is adjusted to cause Zener diode CR5 to conduct whenever the unbalance current is in the 10- to 20-percent range. If this level is reached, CR5 conducts turning Q308 on and Q309 off and starting time delay TD6. After the time delay, the latching circuit, consisting of Q2 and Q3, provides a signal to the TBC-trip amplifier.

Circuit operation for three or more subsystems. - The load-division protection selected for this system does not provide selective tripping for a two-inverter parallel system because tripping either TBC will effectively isolate the subsystems. However, for three or more paralleled inverters, selective tripping is necessary. Demonstrating how a faulted subsystem can be determined in an n-inverter (n greater than 2) system, an analysis of the simplified parallel-system diagram of figure 13a shows the effects of a faulted subsystem on the voltage developed across the secondaries of each current transformer.

First assume that all sensing C-T's are identical and their exciting currents are negligible. Further assume that only one subsystem (say No. 1) is faulted at a time. This means that I_2, I_3, and I_n are equal. The C-T secondary currents are therefore:

$$I_{s1} = aI_1;\ I_{s2} = aI_2;\ I_{sn} = aI_n$$

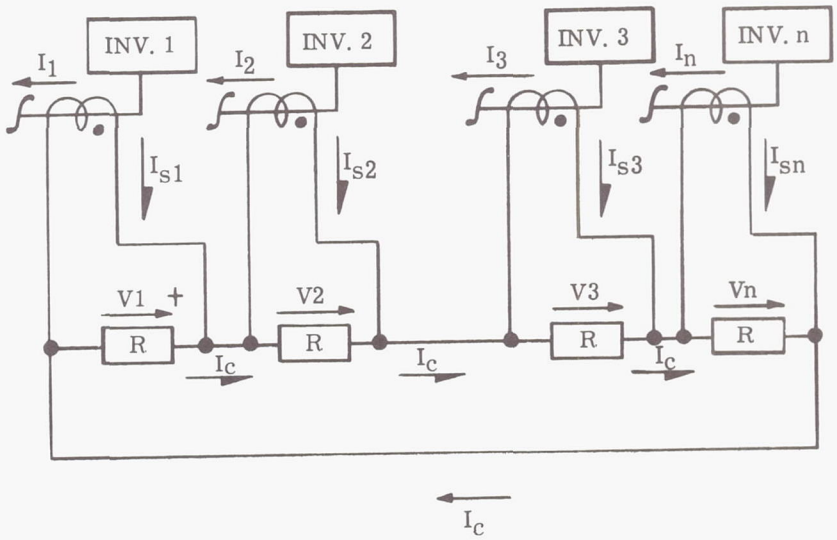
where a = C-T turns ratio.

It follows then that

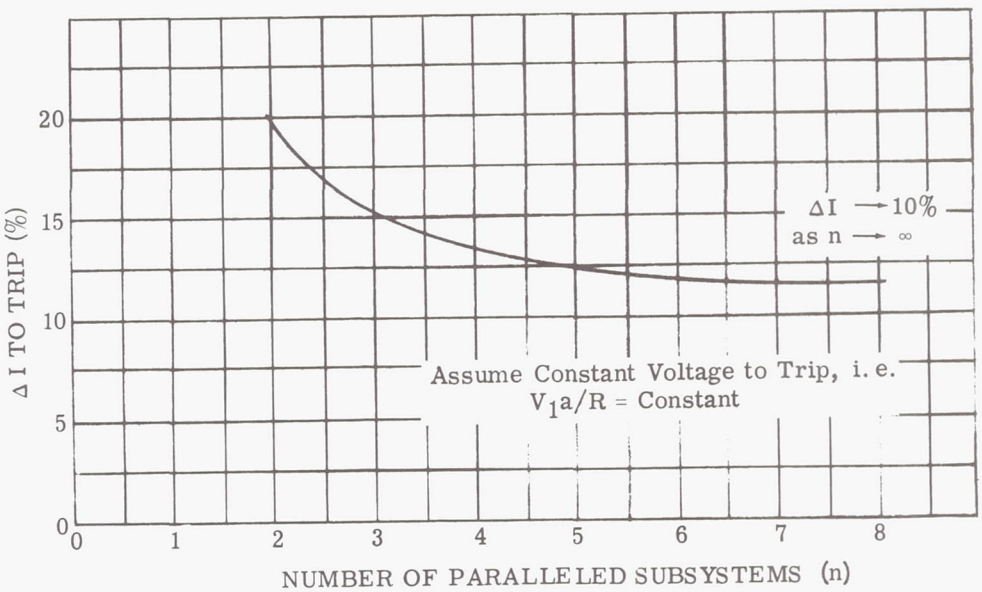
$$I_{s2} = I_{s3} = I_{sn}$$

The circulating current is

$$I_c = V_1/R + I_{s1} = V_2/R + I_{s2} = V_3/R + I_{s3} = V_n/R + I_n.$$



(a) Simplified Inverter Load-Division Sensing Loop



(b) Change in LDP Sensitivity With Number of Paralleled Subsystems

Load Division Sensing Loop & Sensitivity Curve
FIGURE 13.

Therefore,

$$V_1 = V_n + (I_{sn} - I_{s1})R. \tag{6}$$

Now summing the voltages around the loop

$$V_1 + V_2 + V_3 + \cdots + V_n = 0 \tag{7}$$

$$V_1 = R\ (I_c - I_{s1})$$

$$V_2 = R\ (I_c - I_{s2})$$

$$V_3 = R\ (I_c - I_{s3})$$

$$V_n = R\ (I_c - I_{sn})$$

But

$$I_{s2} = I_{s3} - I_{sn}$$

It follows then

$$V_2 = V_3 = V_n$$

and equation (7) becomes

$$V_1 + (n-1)\ V_n = 0 \tag{8}$$

Substituting (8) into (6)

$$V_1 = -\ V_1/(n-1) + (I_{sn}-I_{s1})R$$

which reduces to

$$V_1 = \frac{(n-1)}{n}\ R\ (I_{sn}-I_{s1}) = \frac{(n-1)R}{na}\ (I_n-I_1) \tag{9}$$

$$V_n = -\ \frac{1}{n}\ R(I_{sn}-I_{s1}) = -\frac{R}{na}(I_n-I_1) \tag{10}$$

There are two important points associated with equations (9) and (10). First, the voltage developed across each burden resistor is a function of two variables: the number of systems paralleled and the difference current. Note that if the difference current is zero, both V_1 and V_n are zero. The second point is that V_1 is greater than V_n whenever n is greater than 2. This means that regardless of the magnitude of the difference

current, the voltage developed across the burden of the faulted subsystem is always larger than the voltage developed across the burdens of the unfaulted subsystems. This voltage difference can be used in either of two ways: (1) These voltages may be be applied to inverse time delays. The faulted subsystem time delay will always reach the Zener diode conduction voltage first, and trip the proper TBC because it is the higher voltage. (2) The information may be analyzed using comparator circuits to determine the faulted system. These circuits are discussed further under "Load Division Protection".

There is one other consideration. It was shown that the voltage developed across the burden resistor is proportional to the number of paralleled subsystems. This means that if a LDP circuit is adjusted to trip at a given difference current (say 20 percent of rated) for a system configuration (say two parallel systems), the trip point will vary as systems are added. If the sensing point always trips at the same voltage level, the difference current required to trip will actually decrease. Therefore, the sensitivity of the LDP circuit increases with the number of paralleled subsystems. Figure 13b shows the change in sensitivity. The maximum change in sensitivity is two to one, as n increases from two to infinity. This occurrence is not unique with this sensing circuit or with static inverters. The same problem exists in present aircraft electric power systems.

The problem is circumvented by choosing tolerance limits for the time delays and trip points to include the expected variation due to the number of paralleled subsystems as well as the variations due to environmental factors and component tolerances.

Paralleling Circuits

Requirements. - The inverters used in this study provide three-phase, 400-Hz power by switching four square-wave power stages in a certain sequence. The sequence is determined by the inverter countdown circuit which is driven from the pulses obtained from a 3200-Hz oscillator. This section of the report describes how this basic circuit of the inverter is controlled to meet the requirements of an automatically-controlled, parallel inverter system.

Inverters operating in parallel systems have the same general requirements imposed upon them as do the electromechanical generators. For a better understanding of the requirements and operation of inverters in parallel systems, a brief discussion of the various control functions of an inverter follows.

Figure 1 depicts a three-inverter parallel system. The function of the voltage regulator, as described earlier, is to adjust the terminal voltage of each inverter to maintain equal division of load among the inverters while maintaining the terminal voltage within specified limits. In contrast to the individual prime movers for frequency control in the parallel generator system, the parallel inverter system uses a central reference frequency oscillator. The use of a central reference frequency eliminates the need for feedback loops as is required in the generator system. A more important consideration with respect to paralleling inverters is that the system with a central reference frequency can be synchronized by simply bringing the inverter voltages into the proper phase relationship. This fact makes the automatic synchronization technique more attractive than the automatic paralleling technique generally used in parallel electromechanical generator systems.

Relying upon the regulators to maintain the inverter voltage at the proper magnitude, the only condition left for automatic synchronization is the phase relationship of the inverter voltages. The count-down circuits of the inverter are used to synchronize inverters for two reasons: (1) They provide the only intelligence as to the proper phase relationship of inverters in parallel systems, and (2) Unlike an electromechanical generator, the phase angle of the voltage behind the internal impedance of an inverter is easily obtained.

The state of the count-down circuit of figure 3 provides the phase position of a given phase voltage. The flip-flop circuit identified as A is the reference point for each inverter. Through proper interconnections, flip-flop A in each inverter in a parallel system can provide a synchronizing signal to maintain all count-down circuits in phase. This connection serves to provide a restoring condition analogous to the synchronizing torque in paralleled generators.

Four general specification elements for the paralleling circuit are:

(1) The operation of the circuit must be automatic; i.e., the operator need only to apply power to the inverter.

(2) The inverter to be paralleled must be forced into phase with the parallel system such that no frequency disturbance is induced into the parallel system.

(3) The synchronizer must furnish a periodic signal to the parallel system to restore synchronism should it be momentarily lost because of a transient disturbance.

(4) The circuit used to develop the synchronizer circuit should not alter the functioning of the original inverter circuits.

Circuit design. - Several approaches to arriving at a paralleling circuit which meets the four general specifications were analyzed. The most obvious approach, later rejected, was to use the signals developed for the manual paralleling scheme (as described in NASA CR-1224). This signal, while maintaining synchronism when the signals from both inverters were mutually effective, could not be used in a unilateral mode, i.e., one inverter forcing another inverter into phase with itself. The reason this signal is not sufficient to meet requirement 2 is that small delays accumulated in deriving the signal allow a one-count shift (45 degree error for the test inverters). Thus the inverters would not be properly synchronized until the sync signals were mutually effective. The scheme finally chosen circumvents this problem by narrowing the synchronizing signal during initial synchronization. The original synchronizing signal is reinstated after paralleling has been completed to meet requirement 4 of the general requirements.

Figure 14 is a logic schematic of the inverter countdown circuit and the logic functions required in the C/P circuits. Starting with the original synchronizing signal, waveform 10 of figure 15, an improved synchronizing signal will now be generated. The reference transistor selected for this system is transistor Q18A in the countdown circuit. Referring to figure 3, transistor Q18A can switch off only if Q18B, Q18C, and Q18D are on. As discussed in NASA CR-1224, Q18A can switch off only when capacitor C17A is charged in such a manner as to cause the base of transistor Q18A to be negative with respect to ground whenever the clock turns transistor Q4 on. This means that the voltage level at the point between capacitor C17A and diode CR42A must be lower than voltage at the collector of Q4. The collector voltage of Q4 is developed by voltage divider resistors R26 and R27. The logic equation for the statement that Q18A can switch off only when Q18B, Q18C, and Q18D are on can be stated as:

$$BS = Q18A = \overline{Q18B} \cdot \overline{Q18C} \cdot \overline{Q18D} = B \cdot C \cdot D$$

This signal is used to inhibit Q18A and is therefore called a blanking signal, BS. The BS must be applied between capacitor C17A and diode CR42A, figure 3, to inhibit Q18A. Since this signal must be a zero if Q18A is to switch, the following relationship must exist.

$$\overline{BS} = \overline{\overline{Q18B} \cdot \overline{Q18C} \cdot \overline{Q18D}} = \overline{B} + \overline{C} + \overline{D} \qquad (11)$$

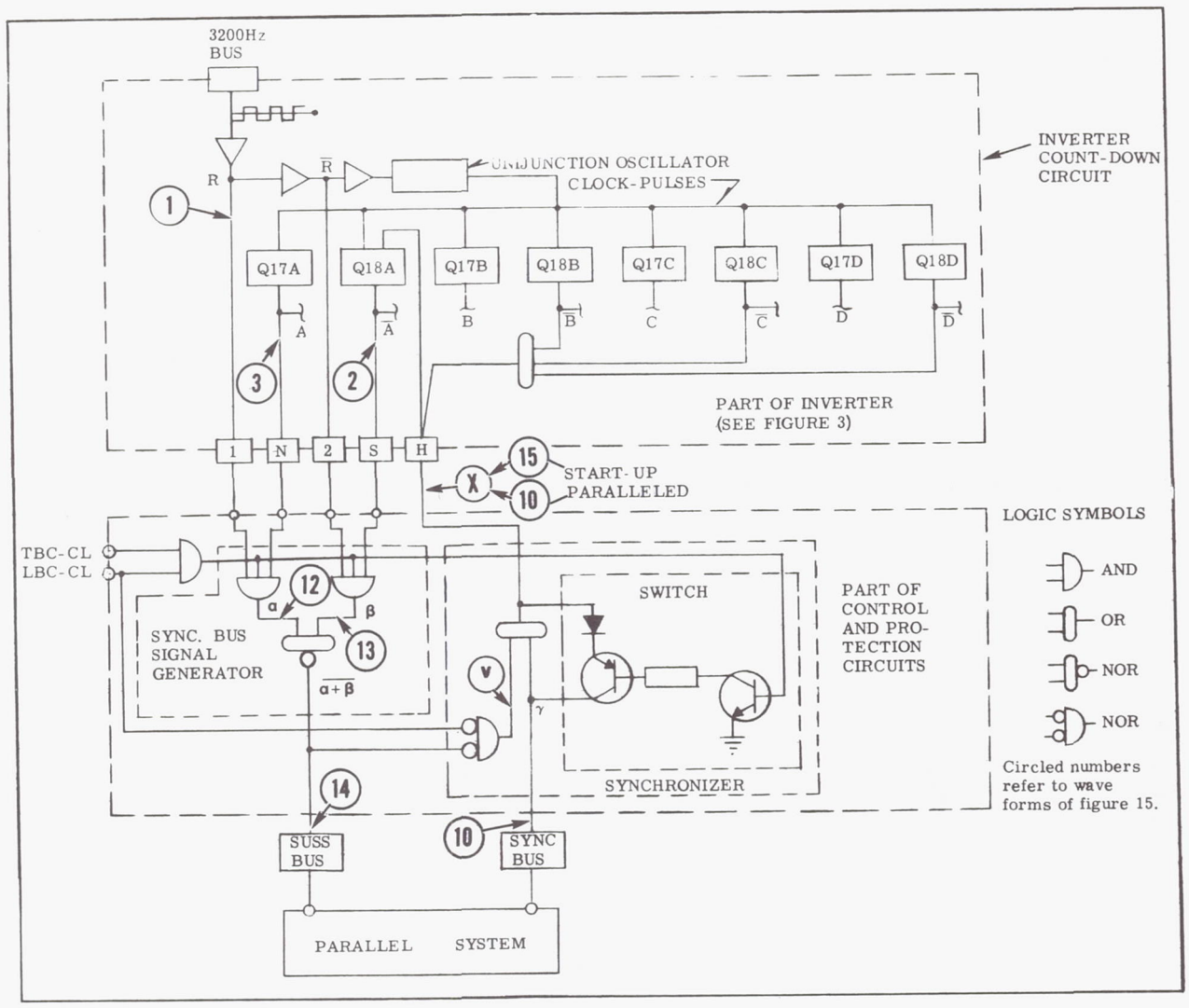


Figure 14. - Logic Circuits for
Inverter Auto Paralleling

The signal defined by equation (11) is shown as waveform 10 in figure 15. The desired signal is shown as waveform 11 in figure 15. Note that waveform 11 is waveform 10 except that the available switching time for transistor Q18A has been reduced from the original 1/1600 second. The switching time available is also centered around the switching point of Q18A. A convenient signal for decreasing the switching time and still maintaining symmetry around the switching point is the voltage of the square-wave oscillator. Note that the available switching time for Q18A can be reduced to 1/3200 second with this signal. The cross-hatched area of waveform 11 corresponds to a positive half cycle

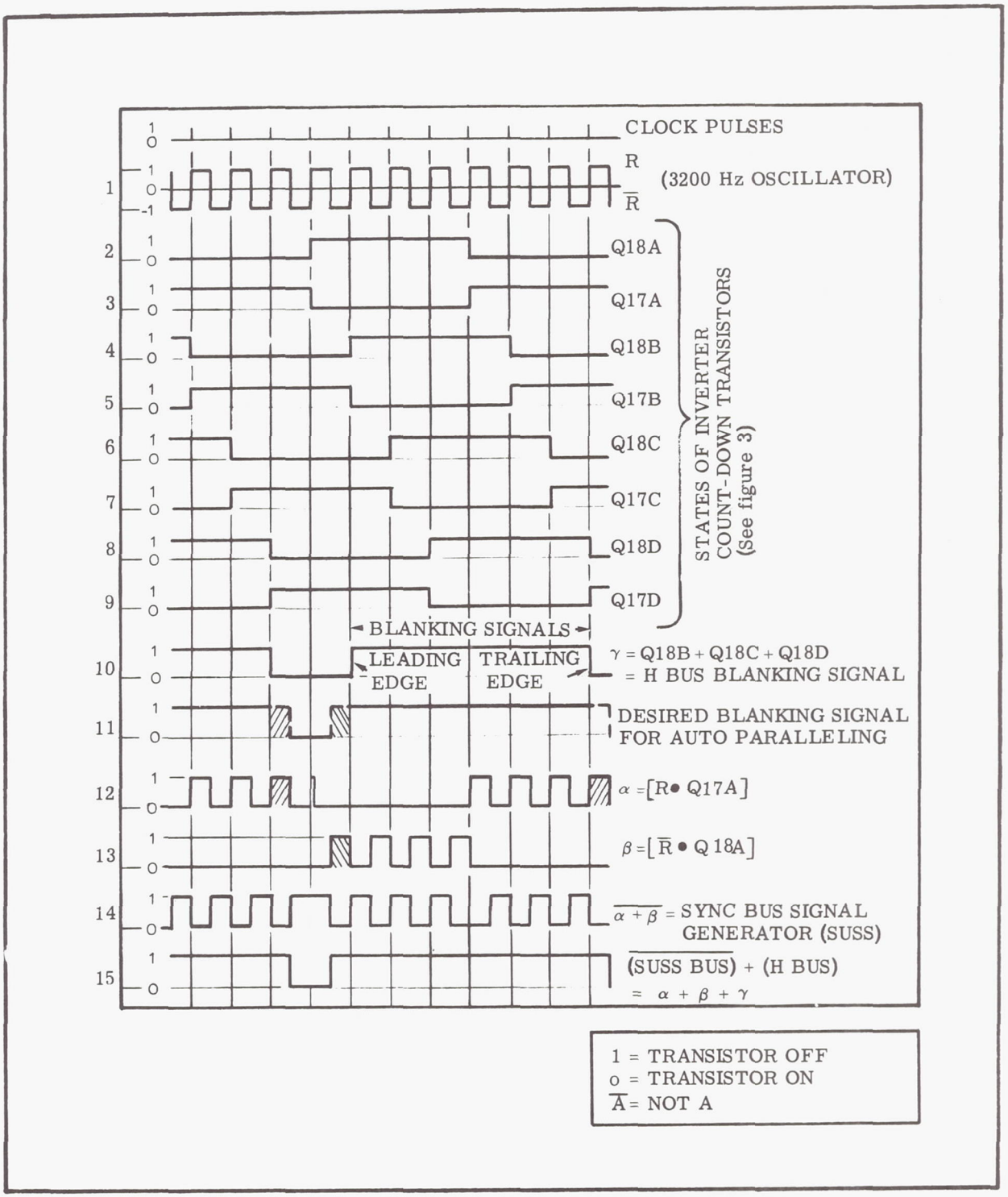


Figure 15. - Derivation of Synchronizing Signal For Auto Paralleling

of the reference oscillator for the leading edge of the blanking signal and to a negative half cycle for the trailing edge. In order to modify equation (11) to obtain waveform 11, some additional information is required. Waveform 2 of figure 15 is the status of Q18A. As stated above, the signal required to lengthen the trailing edge of waveform 10 is the positive half cycle of the reference oscillator. If this signal were added directly to waveform 10, the proper time for Q18A to switch would also be blanked. Note, however, that Q18 is off at the same time the oscillator voltage is positive, and Q18A is on when the undesired positive pulse is present. The logic equation for the extension of the trailing edge is therefore

$$\alpha = A \cdot R = Q17A \cdot R \tag{12}$$

R = Positive half cycle of reference oscillator
α = Signal extending leading edge of the blanking signal

Waveform 12 in figure 15 shows the signal developed from equation (12). The leading edge of the blanking signal can be extended in the same manner. The state of the reference oscillator is negative ($\overline{R}$) and the state of Q18A is position (A) for this condition. The logic equation is

$$\beta = \overline{A} \cdot \overline{R} = Q18A \cdot \overline{R} \tag{13}$$

β = Signal extending the trailing edge of the blanking signal

Waveform 13 in figure 15 shows the waveforms developed from equation (13).

Figure 15 shows that equation (12) develops a narrow blanking pulse. This pulse is caused by the delay in developing the clock pulse and consequently the delay in switching Q18A. This delay also caused the failure of a more simple synchronizing circuit. If waveform 12 were fed back into the inverter blanking signal, an ambiguity would occur because this switching statement implies that Q18 be off if it is to be switched off. Therefore, this statement cannot control the switching of Q18A after the inverter is paralleled.

There are two avenues which may be followed in developing the required synchronizing signal. One is to use waveform 13(β) in combination with waveform 10 (BS) to eliminate the ambiguity. This concept was not used for the paralleled inverter system because the original blanking signal (BS) would be modified. The following configuration was chosen to positively ensure that an on-coming inverter would be in phase with the parallel system

when the parallel operation was completed, i.e., both LBC and TBC were closed. Since α is an ambiguous signal for primary control of the inverter countdown, a means of preventing this signal from reaching the inverter that generates it must be incorporated into the control logic. This can be achieved by employing two busses. Signals composed of α and β from each paralleled inverter are common to one bus. This bus is called the startup sync signal bus (SUSS). The original blanking signal (waveform 10, figure 15) from the paralleled inverters is common to a second bus, designated sync bus. During parallel operation, waveform 10 of each inverter is available through a static switch to maintain synchronism.

In order to startup and parallel reliably, however, waveform 14 of the parallel system (figure 15) must be combined with the sync signal (waveform 10) such that waveform 15 is fabricated To prevent waveform 14 from affecting the operation of the paralleled system, it must be injected into the countdown of the on-coming inverter without being reflected onto the sync bus. This can be accomplished by the OR gate in the synchronizer portion of figure 14. This OR gate in conjunction with the static switch prevents the SUSS from reflecting onto the sync bus. The startup sync bus signal cannot be present at the OR gate after the static switch is closed. This can be accomplished by gating the startup sync signal only when the LBC is not closed. If a NOR gate is placed in series with the OR gate, whose inputs are (a) the waveform 14, and (b) the LBC close signal, the SUSS can be injected into an inverter which is starting up without affecting the parallel system. To prevent the SUSS developed by the on-coming inverter from reaching the startup sync bus, it is blanked by the LBC-CL and TBC-CL signals until the on-coming inverter has been paralleled to the system. The logic equation for the startup sync signal (SUSS) is then

$$SUSS = (\alpha + \beta) \cdot (LBC\text{-}CL) \cdot (TBC\text{-}CL) \qquad (14)$$

Since the inverse of the signal is required, the following relationship must exist.

$$\overline{SUSS} = \overline{(\alpha_1 + \alpha_2) \cdot (LBC\text{-}CL) \cdot (TBC\text{-}CL)} \qquad (15)$$

Waveform 15 of figure 15 is developed from the SUSS and BS (waveform 10) by

$$SYNC = BS + \overline{[SUSS + LBC\text{-}CL]}$$

$$= [(\overline{SUSS}) \cdot (\overline{LBC\text{-}CL})] + BS \qquad (16)$$

Figure 14 is a logic schematic of the complete sync generator and control. The circuit used in the development of the sync control is shown in figure 6.

The circuit operates in the following manner. The sync bus signal generator of figure 6 consists of two AND gates and transistor Q15. Q15 is off if either the LBC-CL or TBC-CL signals are zeros. If both are positive, signals R and A operate through the two AND gates and Q15 to develop the SUSS described in figure 15. R is the 3200-Hz reference oscillator and A is the state of flip-flop A in the inverter countdown circuit.

Transistor Q24 of figure 6 gates the signal from the SUSS bus to the inverter being paralleled whenever the LBC is not closed. Q24 inverts the signal from the SUSS bus by means of the single input AND gate in its base drive. The AND gate is used here to provide a base drive independent of the number of inverters operating. When the system is starting up, Q23 is off and the signal from the sync bus (waveform 10) is available through diode CR327. The SUSS is added to the sync signal through diode CR330. During startup then, the blanking signal injected into the on-coming inverter is waveform 15 of figure 15. When the LBC is closed, Q24 is turned off, removing the signal from the SUSS bus from the blanking signal. The closure of TBC indicates that the on-coming inverter is paralleled and Q23 is turned on by the AND gate driving Q22. The combination of CR326 and Q23 provides a bilateral path for the blanking signal, which is now waveform 10 of figure 15. All inverters have now reverted to the synchronizing signal used in the original parallel inverter study, thus meeting one criteria set forth in development of the automatic synchronizing circuit.

Actual waveforms and further description of the operation of the automatic synchronizing features of this system are presented in the later discussion of "System Tests".

The circuit described provides a means of synchronizing inverters during initial application of power to the inverter. Synchronization is maintained throughout the paralleled mode of operation by providing a synchronizing pulse once each cycle. The complexity of the circuit derived in this program is due to the four general specifications set forth at the beginning of this section. Should a new inverter development be initiated, the circuits could be greatly simplified by including a synchronizing criterion to the design of the countdown circuit.

This circuit concept can be used on any inverter that can accommodate a synchronizing signal to maintain a particular phase angle relationship with respect to other inverters. However,

this technique is directly applicable to those inverters operating from a common reference frequency and utilizing countdown circuits to establish when a particular power transistor is to be switched. This circuit would not be applicable to paralleled inverters operating from different frequency references. In this case, the phase angle relationship would have to be maintained by feedback circuits deriving error signals from the sensed phase currents in the load division circuits. (See NASA CR-1224.)

CONVERTER CONTROL AND PROTECTION

Two modes of system operation for the converter system are provided: automatic and manual. Although automatic system operation is the normal mode, manual system operation is provided if the automatic means fails.

A manual override switch, provided for each subsystem, selects the mode of system operation. Selection of either mode of operation for a subsystem prevents the other mode from operating. When the switch is placed in the AUTOmatic position, 28 volts dc is supplied to the automatic control and protection circuits and to a converter control switch. The subsystem is then ready for automatic operation. When the switch is placed in the MANual position, a ground circuit is provided for the trip and close coils of the converter control contactor, the load-bus contactor, and the tie-bus contactor through manually operated switches. In the OFF position, neither automatic nor manual operation is provided. Figure 16 shows the connection of the switches necessary for both automatic and manual system operation.

Manual System Operation

Manual system operation, the secondary mode, provides a means of operating a subsystem independent of the automatic control and protection circuits. During manual operation, the automatic control and protection circuits are not operative.

To operate the system manually, four switches are required in addition to the manual override switch. Figure 16 shows the connection of these switches. Three of the switches are used to control the converter control contactor (S3), the load bus contactor (S4), and the tie bus contactor (S5). Switch S7 is used to interconnect the load-division-control circuit in the converter (NASA CR-1224). To prevent S7 from interconnecting the load division circuits during the automatic mode of operation, S7 is wired through MOS so that the connection is not complete unless MOS is in MANual position.

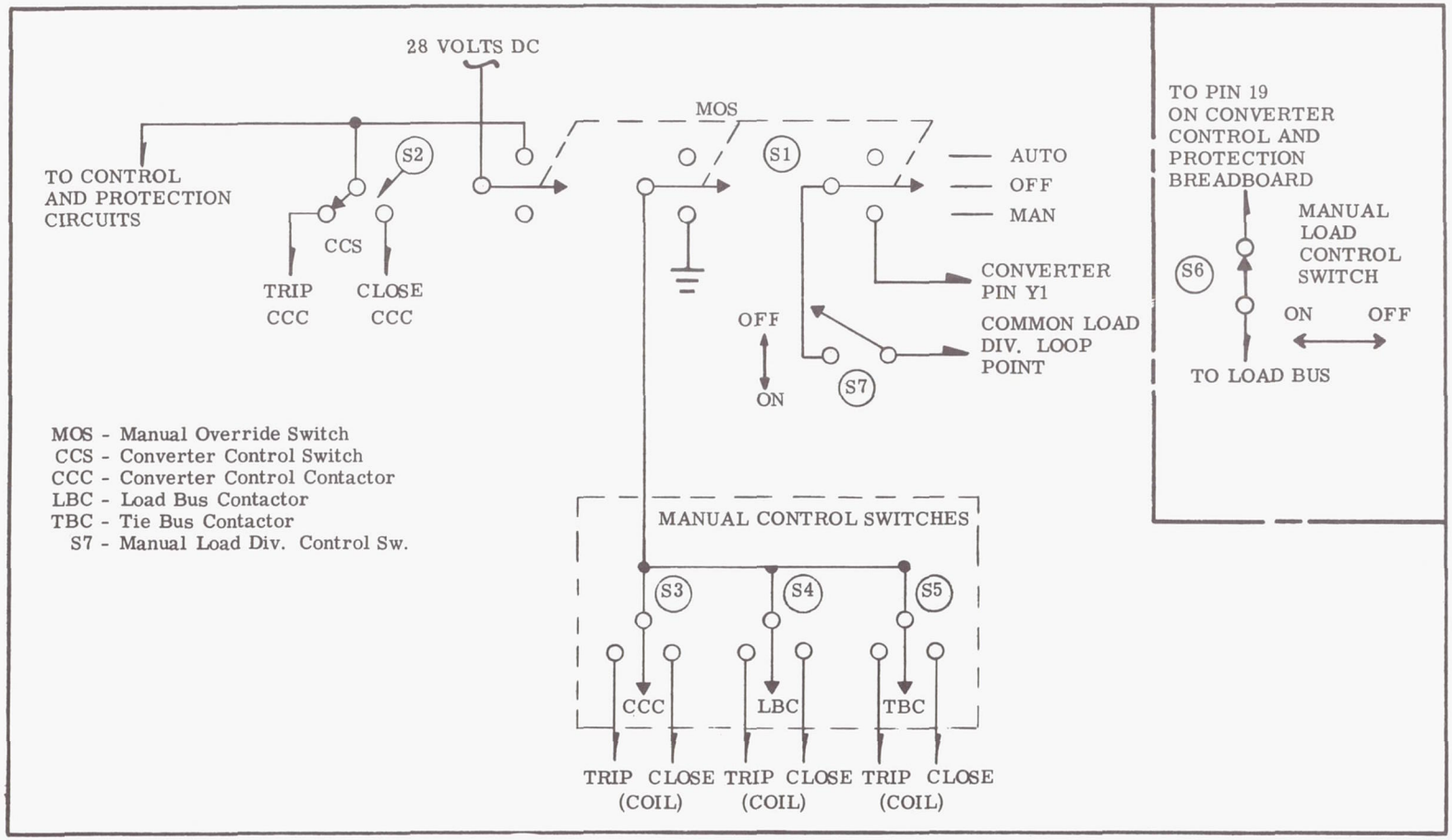


Figure 16. - Converter Switch Connections for Automatic and Manual System Operation

Placing the MOS in the MANual position selects the manual mode of system operation. The converter is then energized by placing the CCC manual control switch in the CLOSE position. After the converter is started, it is connected to the subsystem load bus by placing the LBC manual control switch in the CLOSE position. To connect the subsystem to the tie bus, the terminal voltages of the converter must be of the same magnitude as the converters already connected to the tie bus (unless, of course, no other converter is connected to the tie bus). For these systems, voltage may be within five percent of rated value. After ensuring that the voltages are proper, the TBC manual control switch (S5) is placed in the CLOSE position and the load division control switch, S7, is closed to activate the load-current division circuit within the converter. In the manual mode of operation, the external automatic control and protective functions are inoperative. However, the voltage regulator and load division control circuits located within the converter are operative. Any contactor may be operated manually and in any sequence when the converter is in the manual mode of operation.

One additional manually operated switch (S6) is provided. Its purpose is to isolate the subsystem load bus from the entire system. This switch is called the Manual Load Control Switch in figure 16. The manual load control switch can be operated during either automatic or manual system operation and is provided to connect a particular subsystem converter to the system tie bus without supplying the load bus for that subsystem.

Development of Automatic Control and Protection Functions

Automatic system operation requires only one manual switch (CCS in figure 16) in addition to the manual override switch. The function of the CCS is to connect dc power to the converter by closing the converter-control contactor. The rest of the startup procedure is performed automatically by the control and protection (C/P) circuits.

Automatic control of a parallel converter system includes the assurance that conditions are proper for parallel operation before a converter is paralleled to the system. The automatic protection circuits function to ensure that these conditions prevail while a converter is operating. The function of the protive circuits is not to restore a malfunctioning converter subsystem to normal conditions, but to isolate that portion of the subsystem from the parallel system which is not operating within the nominal limits prescribed for the system. The first section of this report defines the general requirements and approach to protection as it applies to converters in a parallel system.

Figure 1 shows the layout of a parallel converter system with the required sensing points indicated by circled letters A, B, C, D, E, and F. The present discussion integrates these elements into a control and protection network to determine the various normal and abnormal modes of system operation.

The control and protection requirements are first translated into a truth table which specifies a set of circumstances that must exist before a desired action can occur. Circuit implementation is accomplished by providing the necessary sensing circuits to monitor system parameters and then providing the required logic circuits to meet the specifications generated by the truth table. The following section generates each column of the truth table (table IV).

As stated above, there are two requirements for initiating converter startup in the automatic mode of operation: the MOS must be in the AUTOmatic position and CCS must be in the closed position. To prevent a tripped CCS from reclosing, a third condition is imposed: the NO CCS TRIP signal must be present. Column 1 of table IV shows this. This can be stated in symbolic form (see symbol column of table IV) as

$$T1 = A \cdot B \cdot \overline{I}$$

After system startup has been initiated, the output of the converter remains zero for about five seconds. This time delay is a part of the converter circuits. Because the output is zero for an extended time, the ICS must also initiate a time delay within the C/P circuits to allow time for normal startup. This time delay is identified as the no-power-ready time delay (TD1), and it provides seven seconds for converter startup. Time delay TD1 is controlled by two elements: (1) the position of the CCS and (2) the state of the LBC-CLOSE memory.

The LBC-CLOSE signal is used to stop TD1 when the converter starts up normally. TD1 will continue to run unless the CCS is moved to the TRIP position or an LBC-CLOSE signal is obtained.

If a power-ready condition (no abnormal voltage) is not achieved within the 7 seconds, a no-power-ready signal is generated. This signal provides a trip signal to the CCC, a close signal to the TBC, and a lock-out signal to the LBC-CLOSE circuit. This isolates the faulty converter from the system and connects its load bus to the parallel system through the TBC. Column 2 shows the requirements for a no-power-ready signal and column 3 shows the result of this operation. The lock-out of the LBC-CLOSE signal could be accomplished by sending a signal to the LBC-TRIP circuit or by blanking the close signal. The latter method was chosen for a no-power-ready fault on the converter.

Table IV. - Truth Table for Converter Automatic Control and Protection

Independent Variable		Column Number															
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	MOS-AUTO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
B	CCS-CLOSE	1	1														
C	CCS-TRIP																1
D	OV				0					1							
E	UV				0						1						
F	TD1		1														
G	No Power Ready-Memory			1	0												
H	TD2				1												
I	CC-TRIP (memory)	0															
J	LBC-CLOSE (memory)		0			1		1		1	1						
K	LBC-TRIP (memory)				0												
L	DTB (no voltage on tie bus)					1		1									
M	AP						1		1								
N	TD7 - initiated by M						1		1								
O	TBC-TRIP (memory)			0		0	0			0	0						
P	LDC & LDP-TRIP (memory)							0	0							0	
Q	TD3									1	1						
R	DP														1		
S	COCP											1		1			
T	TD4 - initiated by S											1		Ø			
U	TD5 - initiated by T													1			
V	TB OC												1				
W	TD6 - initiated by V												1				
X	LDP															1	
Y	TD8 - initiated by X															1	
Z	TRIP Memory Circuit Reset		0	0						0	0	0	0	0	0	0	Ø
			Startup Fault				Normal Startup			OV Fault	UV Fault	Zone 3 Fault	Zone 2 Fault		Zone 1 Fault	Load Division Fault	Manual Shutdown

Dependent Variable		Column Number															
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T1	CC-CLOSE	1															
T2	No Power Ready Memory		1														
T3	LBC-CLOSE & set memory				1												
T4	TBC-CLOSE			1		1	1			1	1						
T5	CCC-TRIP & set memory			1						1	1			Ø	1		1
T6	LBC-TRIP & set memory			Ø						1	1			1	1		1
T7	TBC-TRIP & set memory											1	1			1	1
T8	LDP & LDC-CLOSE & set memory							1	1								
T9	LDP & LDC-TRIP & set memory									1	1	1	1	1	1	1	1

LEGEND

1 - indicates that the condition must exist to perform the function

0 - indicates that the condition must not exist to perform the function

Ø - indicates that either a 1 or 0 may exist (don't care)

(a)-T(n) is transmission or action resulting from a specific combination of independent variables.

NOTES

1 - System Control and Protection is accomplished on a subsystem basis. A subsystem is considered paralleled when both LBC and TBC are closed.

2 - All functions reading horizontally are OR functions, while all functions reading vertically are AND functions.

3 - See Figure 6 for definition of other terms.

Alternately, if a power-ready condition is achieved within 7 seconds, and lasts for more than 0.20 second (TD2), a signal to close the LBC is generated. TD2 ensures that the power-ready indication was not a transient condition. The output of TD2 initiates a memory circuit since an abnormal voltage condition can remove the signal before the LBC is actually tripped. The output of the memory circuit provides an output until reset by a LBC-TRIP signal (column 4 of table II). The LBC-CLOSE signal stops TD1, closes the LBC, and supplies logic signals to other parts of the control and protection circuits. Closure of the LBC connects the converter subsystem to its load bus providing isolated system operation. This condition is only momentary, however, because the control circuit will attempt to close the tie bus contactor (TBC).

Since closure of the TBC initiates parallel operation, conditions for parallel operation must be satisfied. In the converter system, the system tie bus may be either at zero potential or at rated voltage. Two C/P circuits provide the necessary information to properly parallel. One condition is that no other subsystem is connected to the system tie bus (zero potential). This condition is called a dead tie bus (DTB). The DTB sensing circuit will then provide a signal to close the TBC if the tie bus voltage is nearly zero. To prevent the DTB from prematurely closing the TBC, an inhibiting or blanking signal from the LBC-CLOSE memory is used. Column 5 of table II shows the necessary signals for closing the TBC with a dead tie bus.

The second condition for closing the TBC is that the system tie bus has rated voltage applied to it from other subsystems. The autoparalleling (AP) circuit provides a closing signal under this condition. If both the voltage on the tie bus and the voltage on the load bus are within specified limits of nominal rated voltage, the AP circuit provides a close signal after a short time delay (TD7). TD7 provides 0.20-second delay to ensure that the AP indication was not a transient condition. Column 6 shows the necessary signals for closing the TBC when other subsystems are connected to the tie bus.

Because the closure of the TBC represents parallel operation under normal startup conditions, the load-division control circuit, located in the converter, and the load-division protection circuit must be activated. Therefore, the DTB or the AP signal is used to activate these circuits. Columns 7 and 8 of table IV show the signals necessary to activate the load-division control and protection circuits. Because it is sometimes desirable to close the TBC for reasons other than parallel operation, it is necessary to prevent the activation of these circuits when either the LBC or TBC are tripped. This means that the load-division control and the load-division protection circuit cannot function

unless both the LBC and TBC are closed. Columns 9 through 16 show that any fault condition that trips either the TBC or the LBC also sets a memory circuit which trips the load-division control and protection circuits.

Columns 9 through 16 of table II show how the protection circuits operate for parallel or isolated system operation after startup. As explained previously, abnormal voltage faults on a converter in a parallel system appear as load-division errors but may or may not exceed the overvoltage or undervoltage trip limits. However, in an isolated system, the faults will show up directly, as an abnormal voltage. Since overcurrent faults and load-switching transients can cause temporary abnormal voltage conditions, a time delay is required to prevent false tripping. Because TD1 is too long to provide this function, another time delay (TD3) is used. TD3 does not operate during normal startup because it requires a signal from the LBC-CLOSE (memory) in addition to a signal from either the overvoltage or the undervoltage protection circuit. Columns 9 and 10 show the conditions for an abnormal voltage fault.

The time delays used in the overcurrent protection circuits for Zones 2 and 3 (figure 1) provide two functions. First, the time delays allow time for the secondary protection (fuses, thermal circuit breakers, and the like) to operate. Second, the time delays provide the necessary signals to differentiate between a tie-bus and a load-bus fault. Time delays TD4, TD5, and TD6 provide these signals.

Converter overcurrent sensing (COCP) senses the total current of the converter. If the converter current exceeds 120 percent of rated current, TD4 is initiated, and if the converter overcurrent condition persists beyond TD4, TD5 is initiated.

Current delivered to a subsystem load bus from the tie bus is monitored by the tie-bus overcurrent-sensing circuit (TBOC). When both the tie bus and converter are delivering current to the load bus, the effects of the two currents are additive. However, if the converter supplies both load-bus current and tie-bus current, the effects of the two are subtractive. A detailed description of the tie-bus overcurrent-sensing circuit appears later in "Overcurrent Sensing Circuits."

The tie-bus overcurrent-sensing circuit initiates TD6 when the total current to the load bus is greater than 120 percent of rated. Therefore, if a subsystem load bus is faulted, the tie-bus overcurrent-sensing circuit in the faulted subsystem will indicate a fault; whereas, the paralleled, unfaulted subsystems will indicate only a converter overcurrent.

Overcurrent faults on the tie bus of a parallel system activate all the converter overcurrent-sensing circuits; thus, TD4 is started on all subsystems. Since the converters are delivering current to the tie bus, the tie-bus overcurrent-protection circuits are not activated and TD6 is, therefore, not initiated. To determine the location of the fault, TD4 trips the TBC and starts TD5. TD5 trips the LBC if the fault persists. A tie-bus fault initiates TD4 which starts TD5 and trips the TBC, isolating each subsystem from the tie bus (column 11 of table IV). This removes the converter overcurrent-sensing signal, discharging TD4 and stopping TD5. Each subsystem now operates as an isolated system, i.e., each supplying power to its load bus.

Overcurrent faults occurring on a subsystem load bus also initiate TD4 through the converter overcurrent-protection circuit on each of the paralleled converters. The subsystem with the faulted load bus initiates TD6 through the tie bus overcurrent-protection (TBOC) circuit. TD6 is initiated because the primary winding on the TBOC circuit adds the current from the converter to the current received from the tie bus. Since the remainder of the parallel system sees an apparent tie-bus overcurrent condition, TD6 must be shorter than TD4 to remove the faulted subsystem from the tie bus (column 12). This sequence, therefore, removes the overcurrent condition stopping TD4 on the remainder of the parallel system. TD4 of the faulted subsystem continues to see the overcurrent condition. The signal from TD4 to trip the TBC may be provided but will have no effect on system operation since the TBC has already been tripped by TD6. TD4 initiates TD5 which, when elapsed, trips the LBC (column 13). The faulted load bus is thus isolated from the parallel system and the converter which normally supplies the load bus. Since the converter itself is not faulted but is prevented by the tripped LBC from supplying a load, the converter control contactor (CCC) may be tripped or left closed. A "don't care" or "PHI" condition is thus established.

The truth table requirements for a Zone 1 overcurrent fault and for a load-division fault (columns 14 and 15) may be obtained directly from the earlier discussion "Control and Protection for Paralleled Static Inverters and Converters".

To shut down an unfaulted subsystem, the converter control switch provides a trip signal to the CCC, the LBC, and the TBC. These contactor trip signals also trip the load-division control circuit and load-division protection circuits by signals from the LBC and TBC trip memory circuit. Column 16 of the truth table shows this action.

To implement the C/P circuits from the truth table, the logic statements governing each controlled or dependent variable are written from the columns of the truth table. For example, the load-division control close signal (T8) is activated either by column 7 or by column 8. Reading vertically, LDC-CLOSE must have either of the following conditions: (1) MOS in the AUTO position, an LBC-CLOSE signal, a signal from the DTB circuit, and no LDC-TRIP signal; or (2) MOS in the AUTO position, a signal from the AP circuit, a signal from TD7, and no LDC-TRIP signal. This may be written symbolically as:

$$T8 = \text{LDC-CLOSE} = A \cdot J \cdot L \cdot \overline{P} + A \cdot M \cdot N \cdot \overline{P}$$

$$= A \cdot \overline{P} \cdot (J \cdot L + M \cdot N). \qquad (17)$$

Equation (17) says: close the load division circuit only when A and (NOT P) and either (J and L) or (M and N) are present.

Because time delays require sustained signals to cause them to time out, (M·N) may be redefined to be M_n. This is read: signal M after time delay N. Also as in the case of the inverter, signal A indicates that 28 volts is applied to the C/P circuits. Therefore, if A is not present, no other signal can be present. Signal A is therefore understood to exist in the logic diagram and is therefore omitted from the logic statement.

To ensure that the LDC-CLOSE signal is present until either the LBC or TBC is tripped, signal T8 is latched in. Equation (17) then becomes:

$$T8 = [(J \cdot L) + M_n + T8] \cdot \overline{P} \qquad (18)$$

This can be further modified by reduction formulas to become:

$$T8 = \overline{\overline{[(J \cdot L) + M_n + T8]} + P} \qquad (19)$$

Equation (19) is shown in the converter control and protection logic diagram (figure 17). The latch or memory circuit used in the converter C/P is a silicon-controlled rectifier (SCR). The details of applying an SCR as a memory circuit are discussed in "Converter Control and Protection Circuit Design".

Another example of circuit implementation is the load-division control trip signal. Columns 9 through 16 are the possible protective functions that must trip the LDC circuit. Noting that columns 9 through 16 also trip either the load-bus contactor or the tie-bus contactor, the LDC-TRIP signal can be simplified by simply taking the LBC-TRIP signal and the TBC-TRIP signal rather

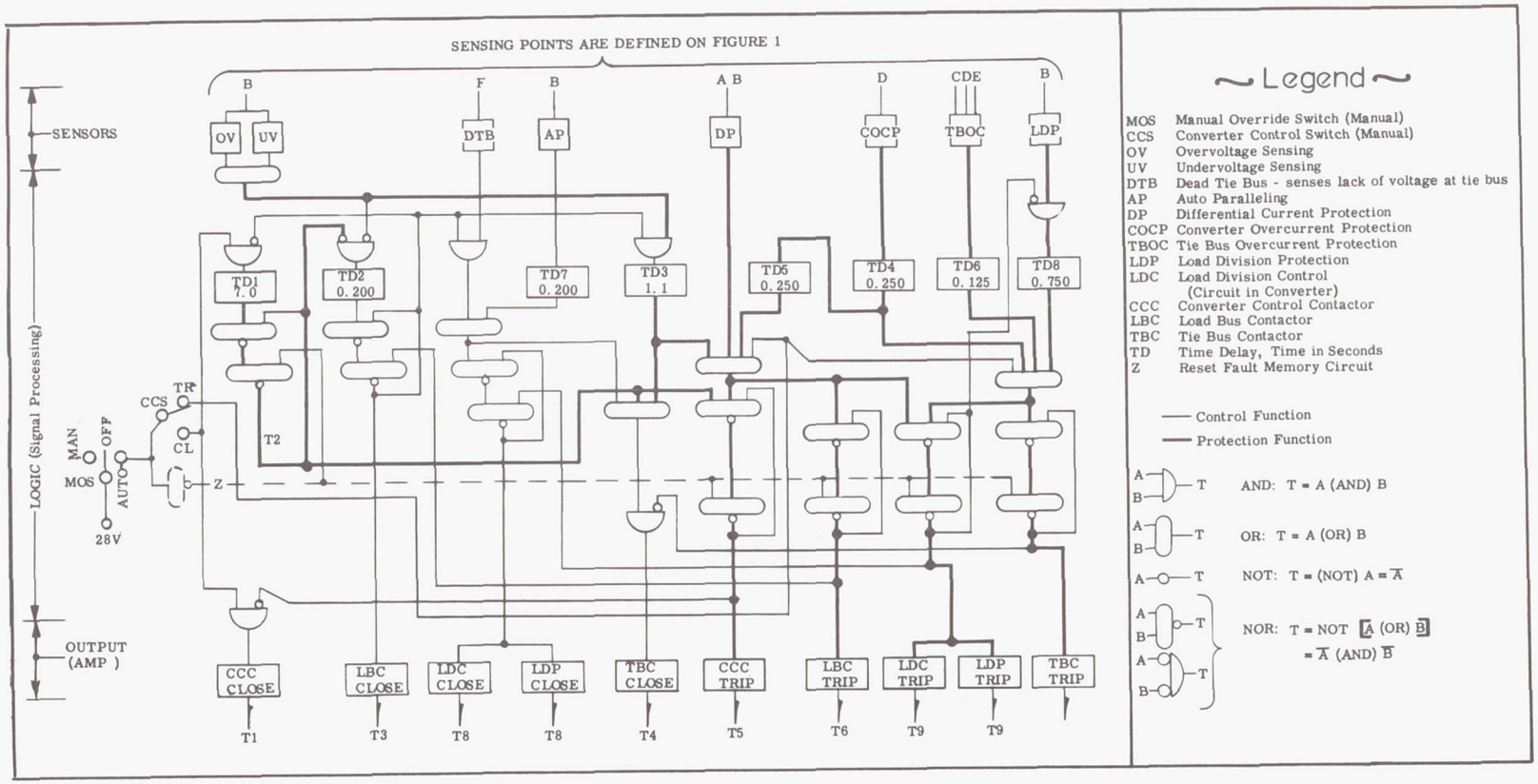


Figure 17. - Converter Automatic Control and Protection Logic Diagram

than the signals which initiate them to generate the LDC-TRIP signal. To ensure the presence of the LDC-TRIP signal until manually reset, the signal is latched-in as in the case of the LDC-CLOSE signal. From the above analysis of the truth table, the load-division control trip signal can be stated as:

$$T9 = \text{LDC-TRIP} = [(\text{LBC-TRIP}) + (\text{TBC-TRIP}) + T9] \cdot \overline{Z}. \qquad (20)$$

Equation (20) can be modified as before to be:

$$T9 = \overline{\overline{[(\text{TBC-TRIP}) + (\text{LBC-TRIP}) + T9]} + Z}. \qquad (21)$$

The reset signal, Z, is shown dotted in figure 17 because Z is derived by removing dc power to the panel by switching MOS to the OFF or MANual position. This approach to resetting the memory is explained in more detail in the later discussion of "Logic Functions".

The rest of figure 17 is generated using the same approach as the examples just given. The final form of each equation is listed in table V. The design of each of the sensing and signal processing circuits is described in the following section.

CONVERTER CONTROL AND PROTECTION CIRCUIT DESIGN

This section provides an operational description of how each sensing, logic, and output function operates, the need for each type of circuit having been established. Figure 18 is a schematic diagram of the complete converter control and protection circuit.

Regulated Direct Current Power Supply

The operation of this circuit was previously described under "Inverter Control and Protection Circuit Design." The shunt regulator consists of resistor R42 and Zener diode Z20.

Logic Functions

Five basic types of logic functions are used throughout the control and protection circuits of the converter system. The first four logic functions were previously described under "Inverter Control and Protection Circuit Design." The latching circuit - memory logic is described below.

Table V. - Logic Equations for Inverter Control and Protection

Column Number in Truth Table	Dependent Variable	Final Equations (a) (See table 4 for symbol definitions)
1	T1	$A \cdot B \cdot \overline{I}$
2	T2	$\overline{\overline{[B \cdot \overline{J}]_f + T2} + Z}$
4	T3	$\overline{\overline{[(\overline{D+E}) \cdot \overline{G}]_h + T3} + K}$
3, 5, 6, 9 & 10	T4	$\{I + (J6) + M_n + [(D+E) \cdot J]_q\} \cdot \overline{O}$
3, 9, 10, 13, 14 & 16	T5	$\overline{\overline{I + [(D+E) \cdot J]_q + S_u + R + (A \cdot C) + T5} + Z}$
9, 10, 13, 14 & 16	T6	$\overline{\overline{[(D+E) \cdot J]_q + S_u + R + (A \cdot C) + T6} + Z}$
11, 12, 15 & 16	T7	$\overline{\overline{S_t + V_w + [X \cdot \overline{P}]_y + (A \cdot C) + T7} + Z}$
7 & 8	T8	$\overline{\overline{(J \cdot L) + M + T8} + P}$
9, 10, 11, 12, 13, 14, 15 & 16	T9	$\overline{\overline{[(D+E) \cdot J]_q + S_t + V_w + S_u + R + [X \cdot \overline{P}]_y + (A \cdot C) + T9} + Z}$

a - Lower-case subscripts indicate that a time delay, corresponding to the CAP letter of table 4, must time-out before the fault signal is received.

Latching circuit - memory logic. - The converter control and protection logic requires several memory or latching circuits to ensure certain signals even though their initiating conditions have disappeared. The latching feature of the controlled rectifier, SCR, provides this function. Once a SCR has been turned on, the gate has no further control over it. One application for the memory is the contactor trip signals. To prevent contactor cycling, a trip signal gates a SCR on, grounding all contactor close signals. The lockout circuit is used for the CCC, the LBC, and the TBC. Figure 19 shows the circuit.

The contactor close signal is processed through Q1 and Q2. When either A or B is present, transistor Q1 is on and Q2 is off, thus supplying a signal to point 2 through R2 and R3. This energizes the contactor close coil.

Should a trip signal occur at either C or D, the contactor trip coil is energized through R5. At the same time, CR1 is turned on through R4. With CR1 on, point 2 is grounded until the current through CR1 falls below the holding current. This is accomplished when dc power is removed by placing the MOS in the OFF or MANual position. Signals C and D no longer have control of CR1.

The logic diagram and logic equations for the contactor trip and close circuit are shown in figure 19. Note that the effective loss of gate control is shown by the feedback of signal T2 to the first NOR gate in the section labeled memory. This is also shown in the logic equation for T2 which implies that T2 is available even though C and D are removed so long as the RESET signal is not present. Reset is noted by the removal of the 15-volt power supply.

The memory portion (SCR and gate drive) of this circuit is also used to turn on and turn off the transistor controlling the load-division control and protection circuits and circuits in the power-ready circuit. It is seen that the single SCR performs the function of a two-transistor flip-flop or memory circuit.

Contactor Trip and Close Amplifiers

The circuits used to provide control of the subsystem contactors are shown in figure 18 in the portions of the circuit marked CCC control, LBC control, and TBC control. The circuits are basically the same, differing only in the number of input signals.

The operation of the LBC-control circuit is as follows:

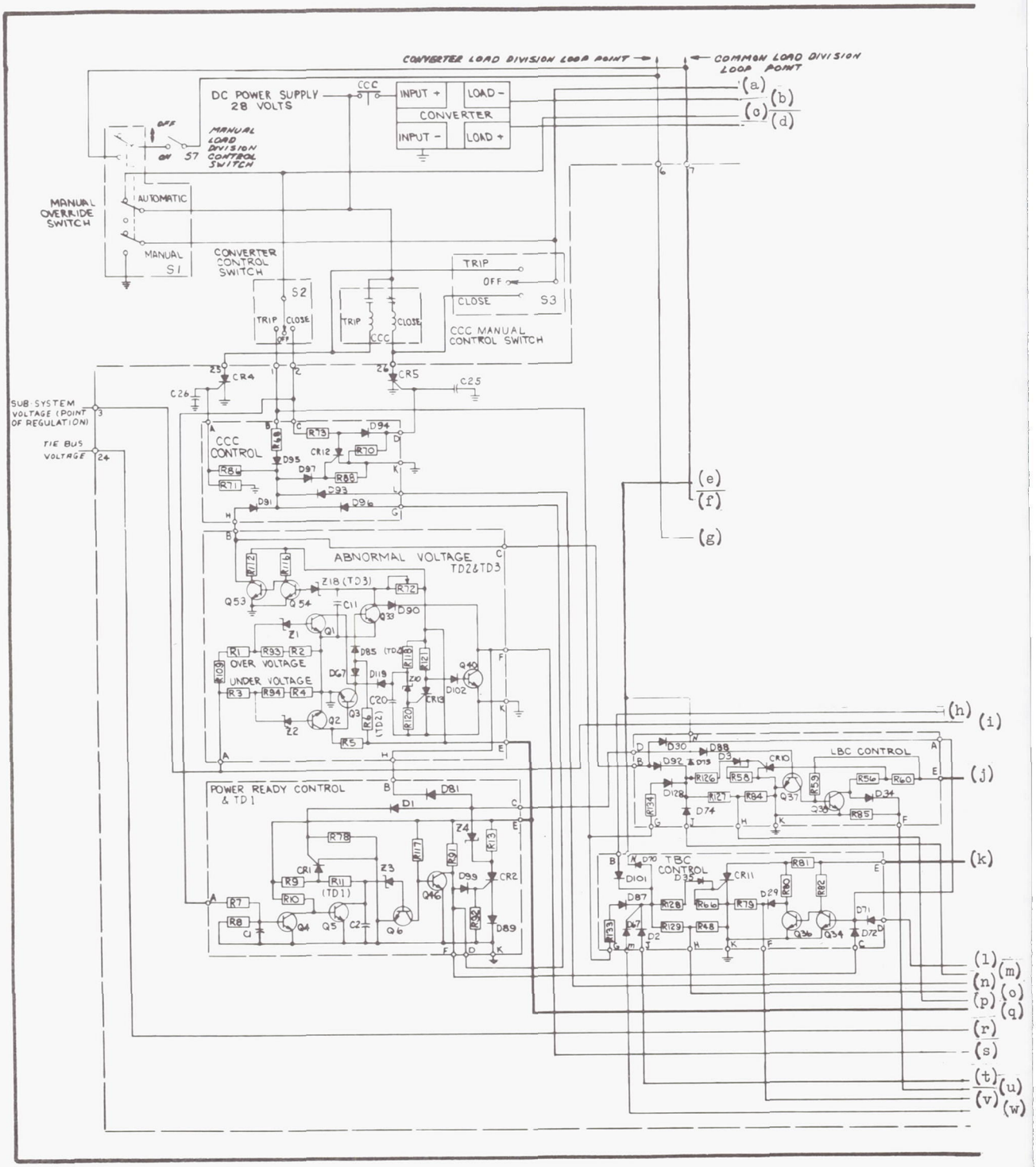


Figure 18. - Paralleled Converters Control and Protection Circuit Schematic

(Con't next page)

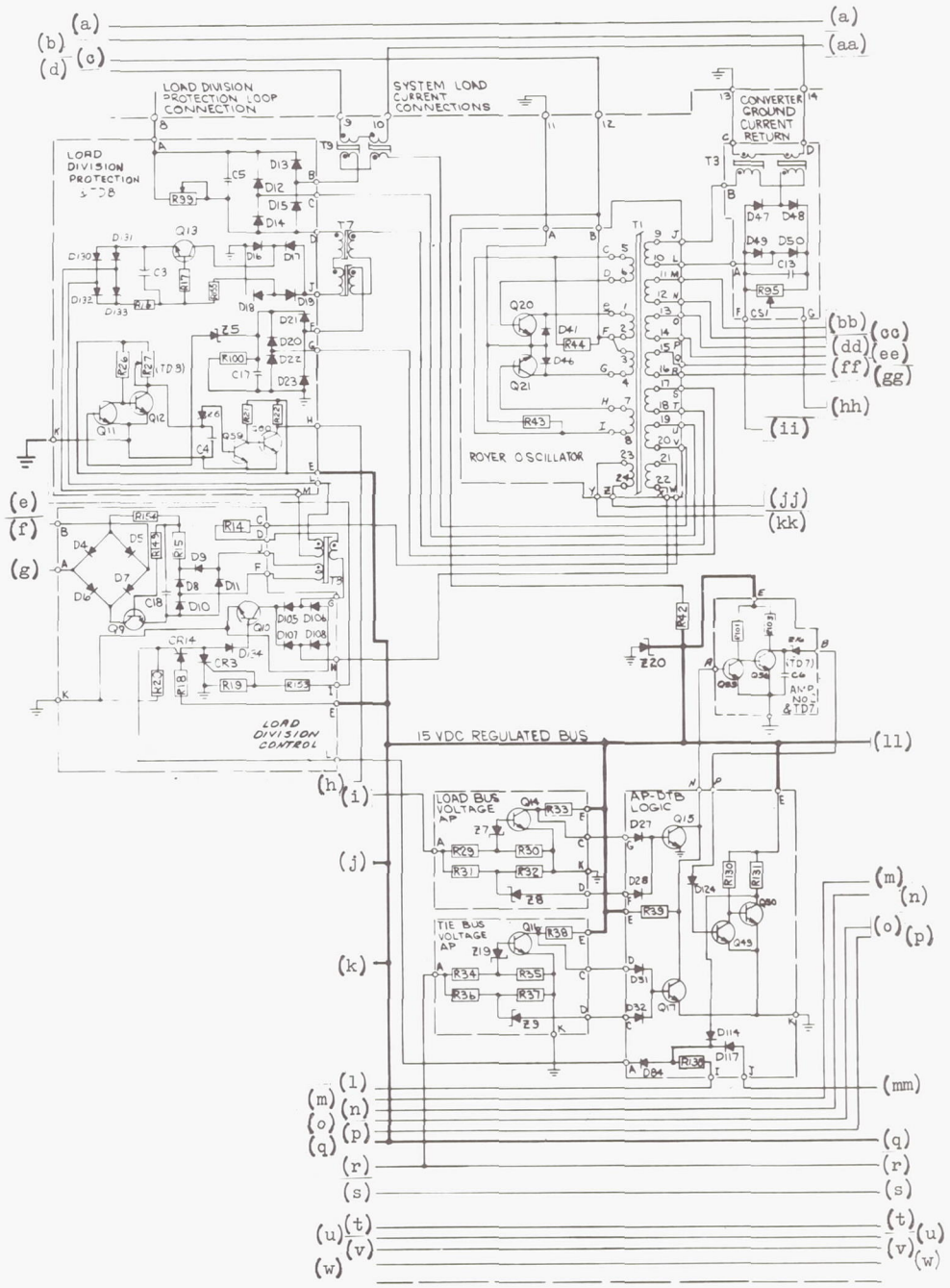


Figure 18. - Continued

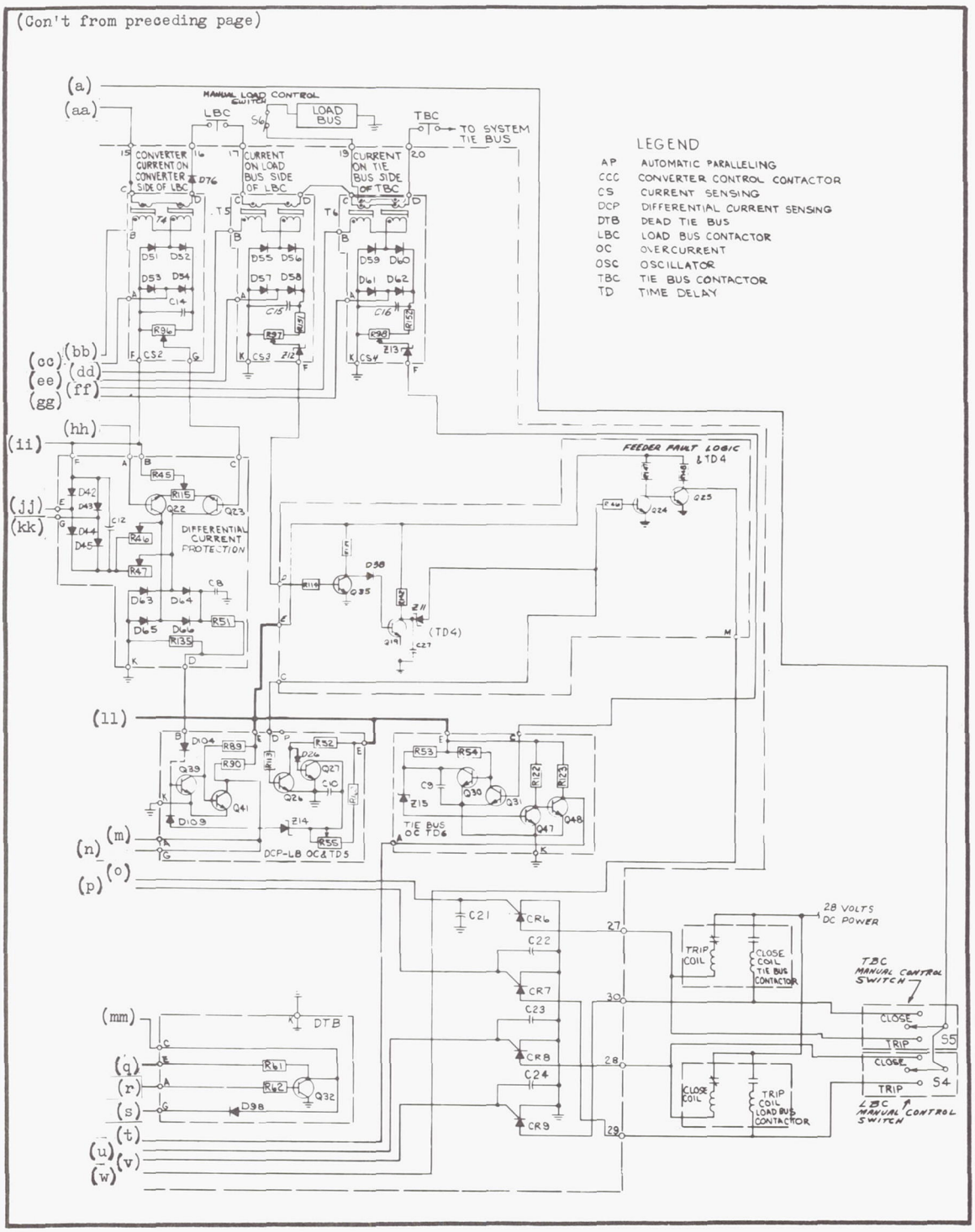


Figure 18. - Continued

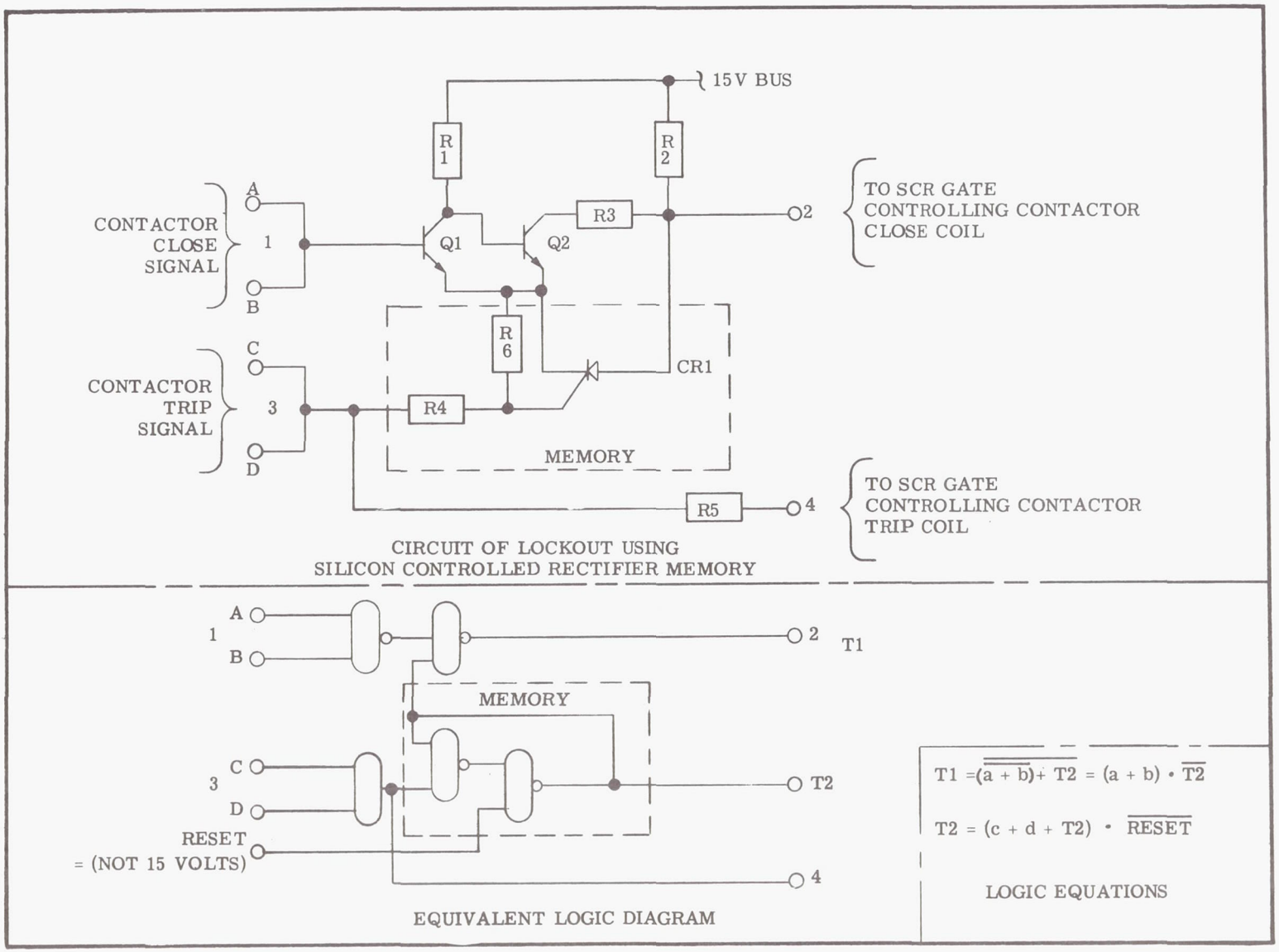


Figure 19. - Latching or Memory Function

When 28 volts are applied to the control and protection circuits, a signal is applied through R59 to the base of Q38, turning it on. With Q38 turned on, the signals through R56 and R60 are prevented from appearing at pin F. When the LBC is to be closed, a signal appears at pin D. This signal is applied through D88 to the base of Q37 turning it on. With Q37 on, Q38 is turned off and an output signal is applied through D34 to pin F. The voltage at pin F is then applied to the gate of CR8, energizing the LBC close coil.

Signals to trip the LBC appear at pins J, G, or B. These signals and diodes D92, D128 and D74 constitute an OR circuit, i.e., any of these signals provide a gating signal to CR7 through R127. Turning CR7 on energizes the trip coil of the LBC. Simultaneously, the trip signal gates CR10 on through R126 and D3. With CR10 turned on, the signals appearing at pin F are shunted to ground, through R60. CR10 provides a latching or memory to prevent the LBC from closing. CR10 remains on until reset by placing the MOS in the manual position (removing power supply voltage). An additional signal is provided at pin N through D73. This signal is applied to pin I on the load-division control board to deactivate the load-division control and protection circuit.

The input signals to close the TBC are applied at pins C, D, and P of the TBC control board while signals to trip the TBC are applied at pins B, G, J, and M.

The converter control contactor is closed by placing the converter control switch in the ON position. Signals to trip the converter contactor are applied to pins B, G, H, and L of the CCC control board.

Abnormal Voltage Sensing Circuits

The abnormal voltage sensing circuit is shown in figure 18 in the portion labeled abnormal voltage.

Subsystem voltage is sensed at the point of regulation. The point of regulation is point B of figure 1. The voltage is applied to two resistive, voltage-divider circuits from pin A on the abnormal voltage board. One voltage divider detects system overvoltage conditions while the other detects undervoltage conditions.

Overvoltage is detected by applying system voltage across the voltage divider consisting of R109, R1, R93, and R2. An output voltage proportional to the system voltages is provided by

the tap between R1 and R93 and is compared to the reference Z1. When the system voltage exceeds 168 volts (nominal voltage is 153 volts), the output voltage of the voltage divider exceeds the breakdown voltage of Z1 and provides a base signal to Q1, turning it on. This shunts the signal normally supplied to the base of Q33, from the 15-volt regulated dc bus through R6 and D85 to ground through D67, turning Q33 off. With Q33 turned off, the signal normally shunted to ground through R72 and Q33 is applied to C11 through R72. The combination of R72 and C11 operating from the 15-volt regulated dc bus provides a fixed time delay, TD3. When the voltage across C11 exceeds the breakdown voltage of Z18, a signal is supplied to the base of Q54, turning it on. The signal normally supplied to the base of Q53 through R116 is shunted to ground through Q54, turning Q53 off. This provides a signal to pins B and C of the abnormal voltage protection circuit through R112. This voltage is applied to the CCC, LBC, and TBC control circuits.

Undervoltage is detected by applying the system voltage across the voltage divider consisting of R3, R94, and R4. An output voltage, proportional to system voltage, is provided by the tap between R3 and R94. This output voltage is compared to the reference Z2. When the system voltage exceeds 138 volts, this output voltage exceeds the breakdown voltage of Z2 and provides a signal to the base of Q2 turning it on. This shunts the signal supplied to the base of Q3 through R5 to ground keeping Q3 off. A signal is then supplied to the base of Q33 through R6 and D85 turning it on if an overvoltage condition does not exist and the signal is not shunted to ground through Q1.

When the system voltage is less than 138 volts, the output voltage of the voltage divider is less than the breakdown voltage of Z2. No signal is provided to the base of Q2, and it turns off, which turns Q3 on. The base signal to Q33 is shunted to ground by Q3 through R6 and D67 turning Q33 off. This starts TD3 as in the case of an overvoltage.

Paralleling Circuits

Dead-tie-bus circuit. - The circuit used to provide dead-tie-bus protection is shown in figure 18 in the portion of the circuit marked DTB.

The system tie-bus voltage is applied to pin A of the DTB circuit from pin 24 of the breadboard. This signal is applied to the base of Q32 through R62. If the signal at pin 24 is less than 5.0 volts, the voltage at the base of Q32 is not sufficient to turn it on. With Q32 off, a signal is provided at pin C through

R61 from the 15-volt regulated bus. This signal is applied to pin J of the AP-DTB logic board where signals are applied through D117 to pins A and I which activate the load-division control and protection circuits and provide a close signal to the TBC control board.

If the system tie-bus voltage exceeds five volts, the voltage at the base of Q32 is sufficient to turn Q32 on. With Q32 on, the signal normally provided to pin C through R61 is shunted to ground and no signal is provided to pin C of the DTB board.

A lockout of the dead-tie-bus circuit, which operates in conjunction with power-ready protection, is provided to prevent its operation until a power-ready condition exists. If a power-ready condition does not exist, Q40 on the abnormal voltage protection board is on. This shunts the dead-tie-bus signal supplied to pin C to ground, through D98 and pin G on the DTB circuit board and Q40 on the abnormal voltage board. When a power-ready condition is reached, Q40 is turned OFF. This removes the lockout signal and provides a signal to pin C of the dead-tie-bus circuit board.

Automatic paralleling circuit. - The circuits used to provide automatic paralleling are shown in figure 18 in the portion of the circuit marked load bus voltage AP, tie bus voltage AP, DTB, and AP-DTB logic. The function of these circuits is to determine whether the quality of power on either side of the TBC is proper for paralleling. The load-bus and tie-bus voltage AP circuits ensure that the on-coming converter is properly paralleled to a tie bus that already has operating converters connected to it. The DTB circuit allows the TBC to be closed when no other converter is connected to the tie bus. The AP-DTB logic circuit provides the signal to operate the tie-bus contactor.

The subsystem voltage, sensed at the point of regulation, is applied to pin A of the Load Bus Voltage AP Circuit. This voltage is applied to two paralleled voltage dividers consisting of R29, R30, R31, and R32. The combination of R29 and R30 is used to sense undervoltage conditions (voltages less than 138 volts), and R31 and R32 is used to sense overvoltage conditions (voltage greater than 168 volts).

An output voltage proportional to the subsystem voltage is provided by a tap between R29 and R30 and compared to the reference Zener diode, Z7. When the subsystem voltage exceeds 138 volts, the breakdown voltage of Z7 is exceeded and a base signal is supplied to Q14, turning it on. With Q14 turned on, the signal normally supplied to the base of Q15 (through R33 and D27) is shunted to ground through Q14. This turns Q15 off. If the

subsystem voltage is less than 138 volts, the breakdown voltage of Z7 is not exceeded, and no base signal is supplied to turn Q14 on. A signal is then supplied to the base of Q15, turning it on.

An output voltage proportional to the subsystem voltage is provided by a tap between R31 and R32. The voltage is compared to the reference Zener diode, Z8. When the system voltage is less than 168 volts, the output voltage does not exceed the breakdown voltage of Z8. No base signal is then supplied to Q15, and it remains off. When the subsystem voltage exceeds 168 volts, the breakdown voltage of Z8 is exceeded, and a signal is supplied through D28 to the base of Q15. This turns Q15 on.

The voltage sensing circuits on the tie bus voltage AP circuit, which sense the tie bus voltage, operate as described above for the load bus voltage AP circuit. The final action is control of Q17. If the voltage conditions required for automatic paralleling have been satisfied, Q15 and Q17 are both turned off. This applies a signal through R39 and D124 to the base of Q55 turning it on. With Q55 turned on, the signal normally supplied to the base of Q56 through R101 from the 15-volt regulated bus is shorted to ground, turning Q56 off. This applies a voltage to C6 through R103 from the 15-volt regulated dc bus. This combination provides a fixed time delay, referred to as TD7, and is required to override transient conditions during which the voltage limits for paralleling would be satisfied momentarily. The voltage across C6 is compared to the reference Z16. When it exceeds the breakdown voltage of Z16, an output signal is supplied to the base of Q49 turning it on. With Q49 turned on, the signal normally supplied to the base of Q50 through R130 is shunted to ground and Q50 is turned off. This provides a signal through R131 and D114 to pin A through D84 and to pin I through R138 to the load-division control and protection circuit boards, activating the load-division control and protection circuits, and to the TBC control circuit board to close the TBC. This establishes parallel operation.

Transductor Current Sensing Circuit

Because some of the protective functions monitor system current, a method of sensing the magnitude of direct current is required. A transductor circuit provides an output voltage proportional to the magnitude of the direct current. The transductor circuit consists of an ac source, two magnetic devices (transductor elements), a full-wave bridge rectifier, a filter capacitor, and a resistive burden. Figure 20 is a schematic diagram of the transductor circuit.

Each of the transductor elements is alternately driven into saturation each half cycle of the Royer oscillator voltage. One

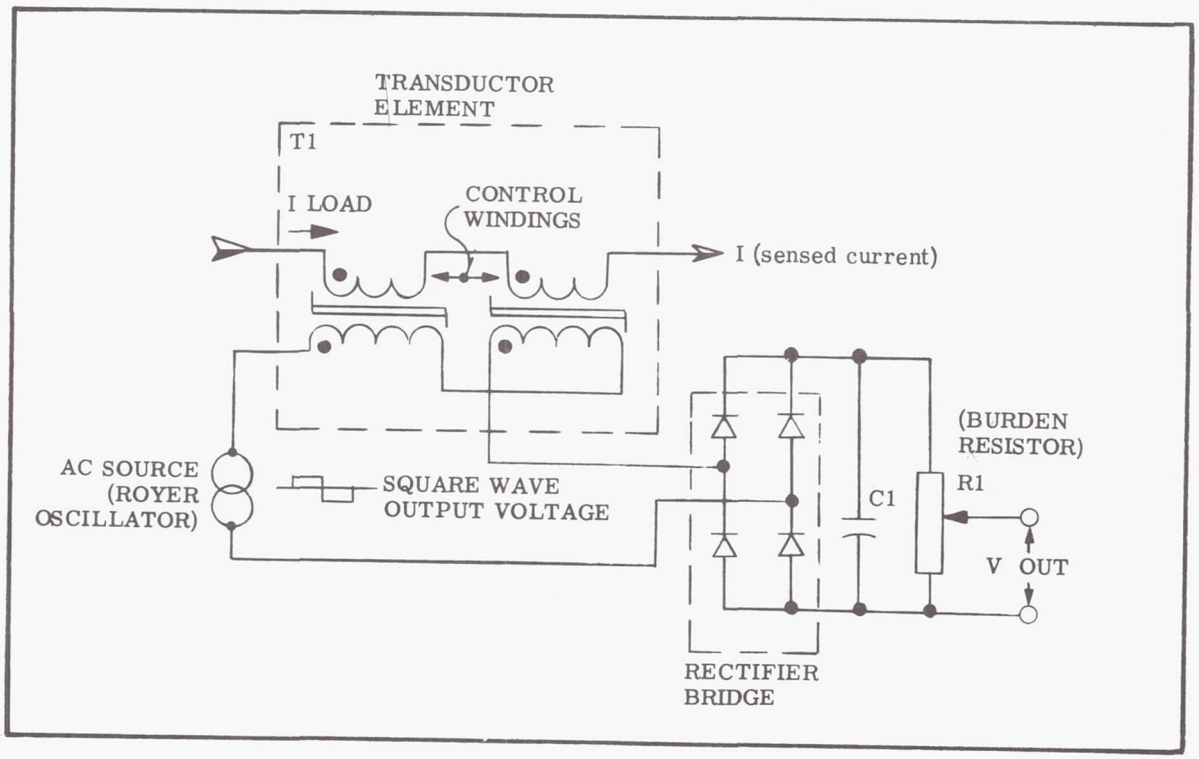


Figure 20. - DC Current Sensing Circuit
(Transductor Circuit)

core will saturate after absorbing some volt-seconds of the applied voltage. With one core in saturation, its control winding appears as a short on the control winding of the remaining core. This reduces its impedance to zero, even though it has not saturated, and the remaining half cycle of the applied voltage appears across the resistive burden. When the applied voltage changes polarity, the action is repeated with the other core being driven into saturation. The voltage that appears across the resistive burden is first converted to a direct voltage by the full-wave bridge, thus providing a direct voltage output.

When direct current is applied through the control windings, the cores are biased so that they will absorb less volt-seconds of the applied voltage. This results in a larger portion of the cycle appearing across the resistive burden and increases the average output voltage of the transductor circuit. This output voltage increases linearly with the magnitude of the direct current in the control windings. When the current through the control windings is large enough, the cores are always in saturation and the output voltage of the Royer appears across the resistive burden. No further increase in output voltage will occur with increased current in the control windings, and this represents the maximum output voltage of the transductor circuit.

Figure 21 shows typical output characteristics of the transductor current-sensing circuit. For more detailed information on the design and operating characteristic of transductor circuits, see Chapter 3 of reference 4.

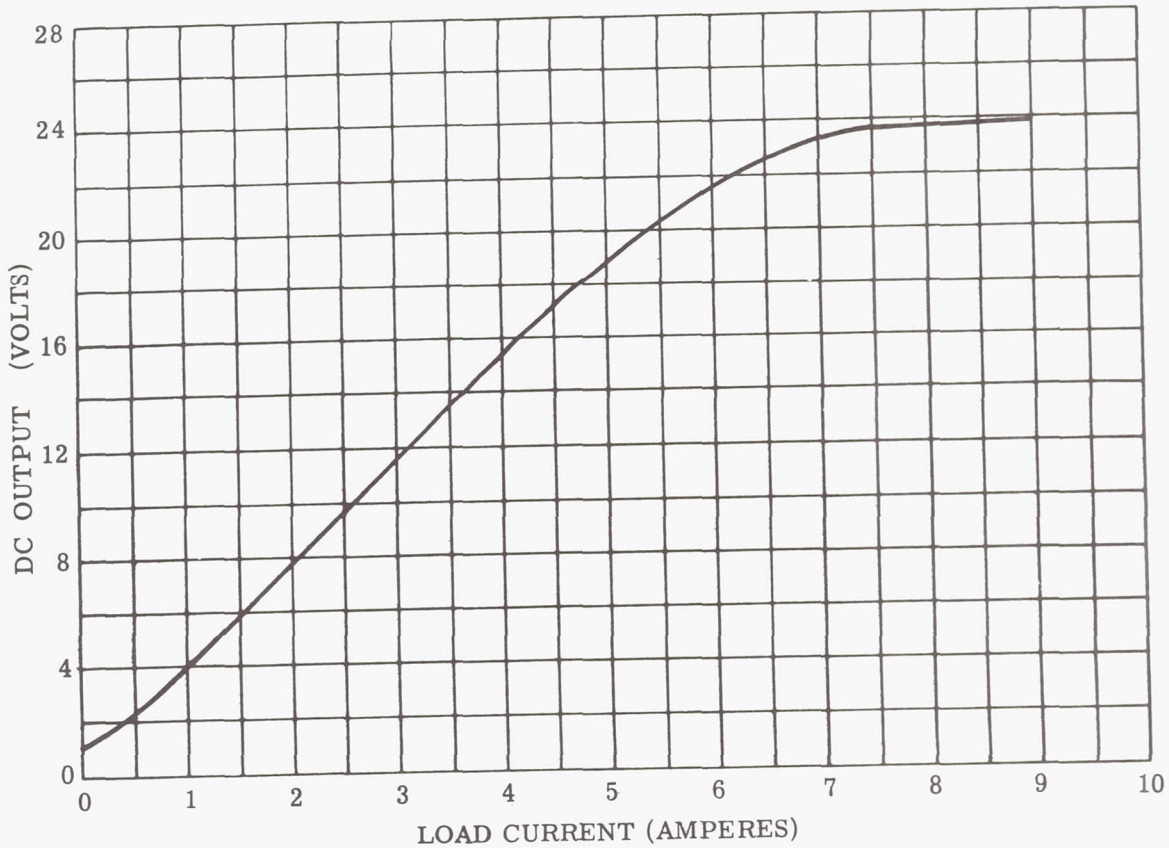


Figure 21. - Typical Current Sensing Circuit Characteristics (Transductor Transfer Function)

The transductor current-sensing circuit was used to sense the magnitude of direct current in differential-current protection, the overcurrent protection, and load-unbalance protection circuits.

Differential Current Sensing Circuit

The purpose of the differential protection circuit is to determine when the current at the load-bus contactor is not equal to the current in the ground return of the converter. The DP circuit protects the subsystem between points A and B of figure 1. Since this portion of the converter subsystem does not normally supply current to loads other than that connected to its load-bus

contactor, any time the ground-return current is not equal to the current leaving the LBC, a fault condition exists. The DP circuit consists of two current sensors (CS1 and CS2 of figure 18) and a comparing circuit (the differential amplifier Q22 and Q23 of figure 18).

The converter ground-return current is sensed by the transductor circuit, CS1, and the current at the load-bus contactor is sensed by transductor circuit, CS2. The output voltage of these two transductor circuits is applied across potentiometers R95 and R96, respectively. R95 and R96 are adjusted to match the output voltages for equal transductor control (load) current.

The transductor sensing circuit is sensitive to current magnitude but is not sensitive to current direction. Therefore, for feeder faults occurring in Zone 1 during parallel system operation, the fault could be supplied equal fault currents from both the converter and the system tie bus. Even though the currents are in opposite directions in the two current sensing circuits, the differential protection circuit would not indicate a Zone 1 fault should the magnitudes be equal. To provide correct operation for Zone 1 faults during parallel system operation, a blocking diode, D76, is connected in the converter output feeder at the LBC to prevent current from flowing into Zone 1 from the system tie bus. This diode is essential for correct operation of the differential current protection circuit during parallel system operation.

The output voltage of CS1 is applied to the base of Q22 on the Differential-Current-Protection board. The output of CS2 is applied to the base of Q23 on the same board. When the voltages applied to the bases of Q22 and Q23 are equal, the transistor collector-to-emitter currents are equal. The voltage drop across R46 is equal to that across R47, and no voltage difference exists between the collectors of Q22 and Q23. The collectors of Q22 and Q23 are interconnected through a steering circuit consisting of D63 through D66, R51 and R135. Capacitor C8 suppresses voltage spikes. When the base signal of one transistor is different from that of the other, the amount of current allowed to flow through each transistor is different. This results in a different voltage drop across the collector resistors R46 and R47, resulting in a voltage difference between the collectors of Q22 and Q23. This voltage difference is proportional to the difference in input voltage to the bases of Q22 and Q23 and is applied to the steering circuit and the voltage divider R51 and R135. An output voltage, provided by a tap between R51 and R135, is applied to the base of Q39 through D104, on the DCP-LB OC TD5 board.

Power from the 15-volt regulated bus is applied through R89 to the base of Q41, turning it on. This shunts the dc power to ground through R90 and prevents any output signal from being

supplied from pins A and G. When Q39 turns on (because of a differential current signal) the signal supplied to the base of Q41 is shunted to ground, turning Q41 off. This provides trip signals to the CCC control and the LBC control circuits through pins A and G.

Overcurrent Sensing Circuits

Converter overcurrent. - The overcurrent protection circuits used to provide Zone 2 and Zone 3 (figure 1) fault protection are shown in figure 18 in the portions of the circuits marked CS3, Feeder Fault Logic, and DCP-LB OC, TD5. The converter load current is sensed by the transductor circuit, CS3. An output voltage proportional to this load current is compared to the reference Zener diode, Z12. When the breakdown voltage of Z12 is exceeded, an output signal is provided to the base of Q35 through R114, located on the Feeder Fault Logic and TD4 board, turning Q35 on and Q19 off. With Q19 off, time delay TD4 is started. If the fault persists beyond TD4, transistors Q24 and Q26 are turned on. With Q24 turned on, Q25 is turned off and a signal through R148 is provided to the TBC control circuit to trip the TBC.

If the overcurrent condition is removed when the TBC is tripped, the signal from the load-bus overcurrent transductor circuit is removed from the base of Q35. This results in Q19 turning on, removing the signal from the base of Q26. This stops TD5 and prevents signals from being supplied to the CCC and LBC control circuits.

However, if the overcurrent condition is not removed when the TBC is tripped, Q35 remains on and TD5 continues to run. If the fault persists beyond TD5, Q39 is turned on and Q41 is turned off. A trip signal through R90 to the CCC and LBC control circuits is provided through pins A and G of the DCP-LB OC TD5 board.

Tie bus overcurrent. - The converter overcurrent sensing circuit senses fault current for both Zones 2 and 3 of a subsystem. To provide coordination between Zones 2 and 3, a second overcurrent sensing circuit for each subsystem is provided. The circuit, called tie-bus overcurrent, is shown in figure 18 in the portion of the circuit marked CS4 and TIE BUS OC TD6. Tie-bus current is sensed on the load-bus side of the tie-bus contactor using transductor T6. To determine the direction of the tie-bus current, the transductor elements contain two control windings. One control winding (B) of transductor T6 is connected between sensing points C and D of figure 1 to monitor the current delivered to the load. The second control winding (A) is connected between

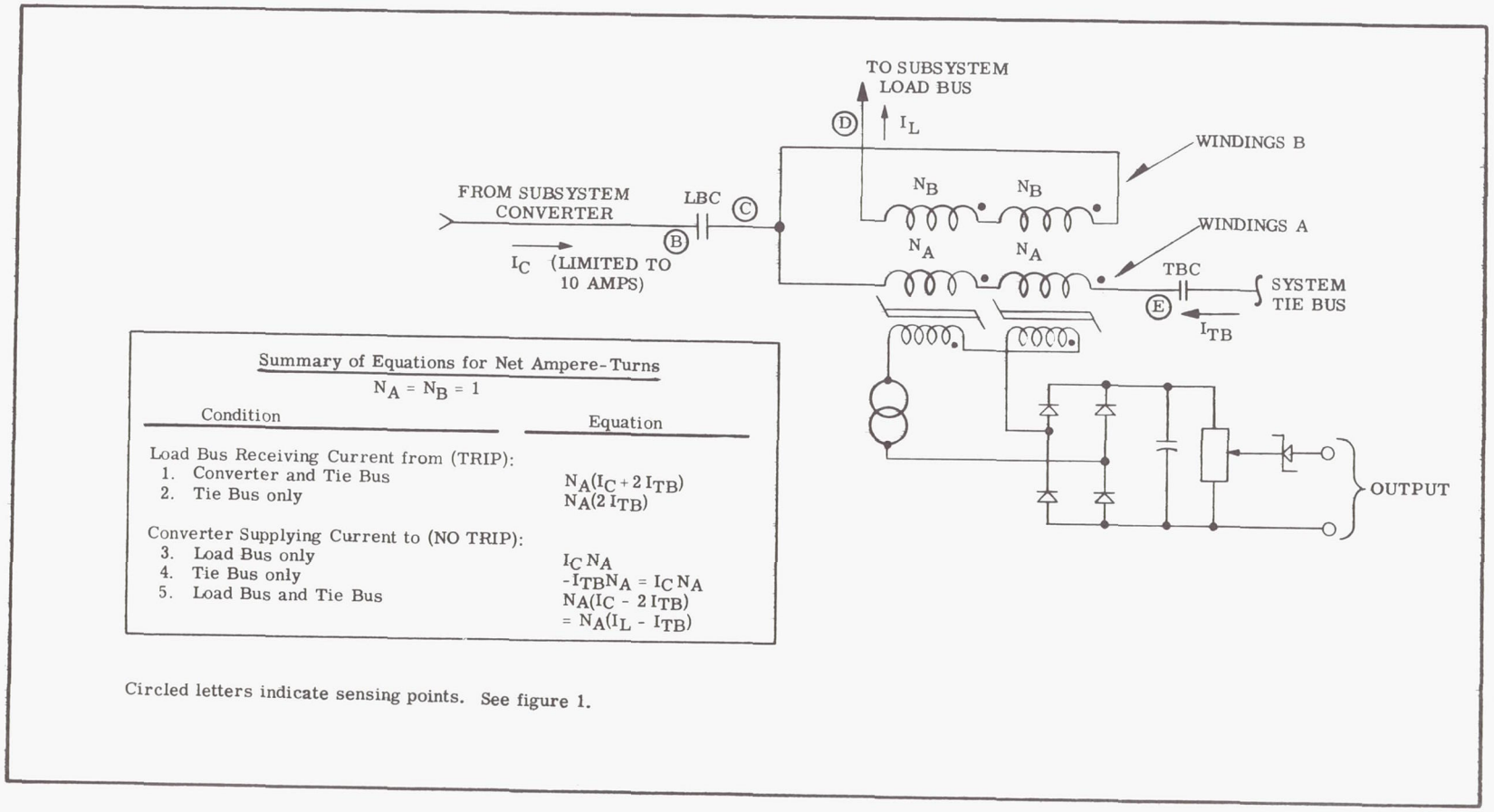
sensing points C and E of figure 1 to monitor the current from the tie bus. Figure 22 shows the two control windings (A and B) and the tie-bus current sensing circuit. Of the five different possible conditions, two must cause the TBC to TRIP while the other three must not. These conditions are listed in figure 22. Control windings A and B are wound so that a load bus receiving current from the system tie bus will add the ampere turns developed in each control winding to achieve a maximum number of ampere turns. The tie-bus overcurrent circuit is adjusted to provide an output signal only when the net ampere turns in the transductor element exceed eleven ($N_A = N_B = 1$). Referring to figure 22 and noting the sense of the currents and the polarity (dots) of the transductor elements, the equation for the total ampere turns is

$$I_L N_B + I_{TB} N_A = (I_C + I_{TB}) N_B + I_{TB} N_A$$

when the load bus is receiving current from both the tie bus and the converter. From this equation it is seen that the TBC will be tripped whenever the tie bus furnishes more than 5.5 amperes ($I_{TB} > 5.5$ amps) to the load bus. This circuit protects the tie bus whether or not the subsystem converter is connected to the load bus, i.e., $I_C = 0$.

This circuit must not trip the TBC when the converter supplies current to either the load bus or the tie bus. Equations 3, 4, and 5 in figure 22 show the net ampere turns developed under this condition. Utilizing the current limiting feature of the converter, equations 3, 4, and 5 show that the TBC will not be tripped if the maximum converter current is eleven amperes or less. Since the converter is limited to two per unit current (10 amperes), the tie-bus overcurrent circuit will not trip for any of the three conditions.

When a tie-bus overcurrent condition exists, the output voltage of the transductor circuit is applied across the voltage divider R152 and R98 (figure 18). Potentiometer R98 provides an overcurrent output signal when the current from the system tie bus to the subsystem load bus exceeds 5.5 amperes. The output voltage of the voltage divider is compared to the reference Zener diode, Z13. When the output voltage exceeds the breakdown voltage of Z13, a signal is provided to the base of Q31, located on the TIE BUS OC, TD6 board, turning it on. With Q31 turned on, the signal normally supplied to the base of Q30 through R54 is shunted to ground, turning Q30 off and starts time delay TD6. If the fault persists beyond TD6, Q47 is turned on and Q48 is turned off. A signal to trip the TBC is provided through pin A of the TIE BUS, OC, TD6 Board. If the fault persists after the TBC trips, the converter overcurrent sensing circuit continues TD4 and TD5 as before.



Summary of Equations for Net Ampere-Turns

$N_A = N_B = 1$

Condition	Equation
Load Bus Receiving Current from (TRIP):	
1. Converter and Tie Bus	$N_A(I_C + 2\,I_{TB})$
2. Tie Bus only	$N_A(2\,I_{TB})$
Converter Supplying Current to (NO TRIP):	
3. Load Bus only	$I_C\,N_A$
4. Tie Bus only	$-I_{TB}N_A = I_C\,N_A$
5. Load Bus and Tie Bus	$N_A(I_C - 2\,I_{TB})$ $= N_A(I_L - I_{TB})$

Circled letters indicate sensing points. See figure 1.

Figure 22. - Tie-Bus Overcurrent Sensing Circuit

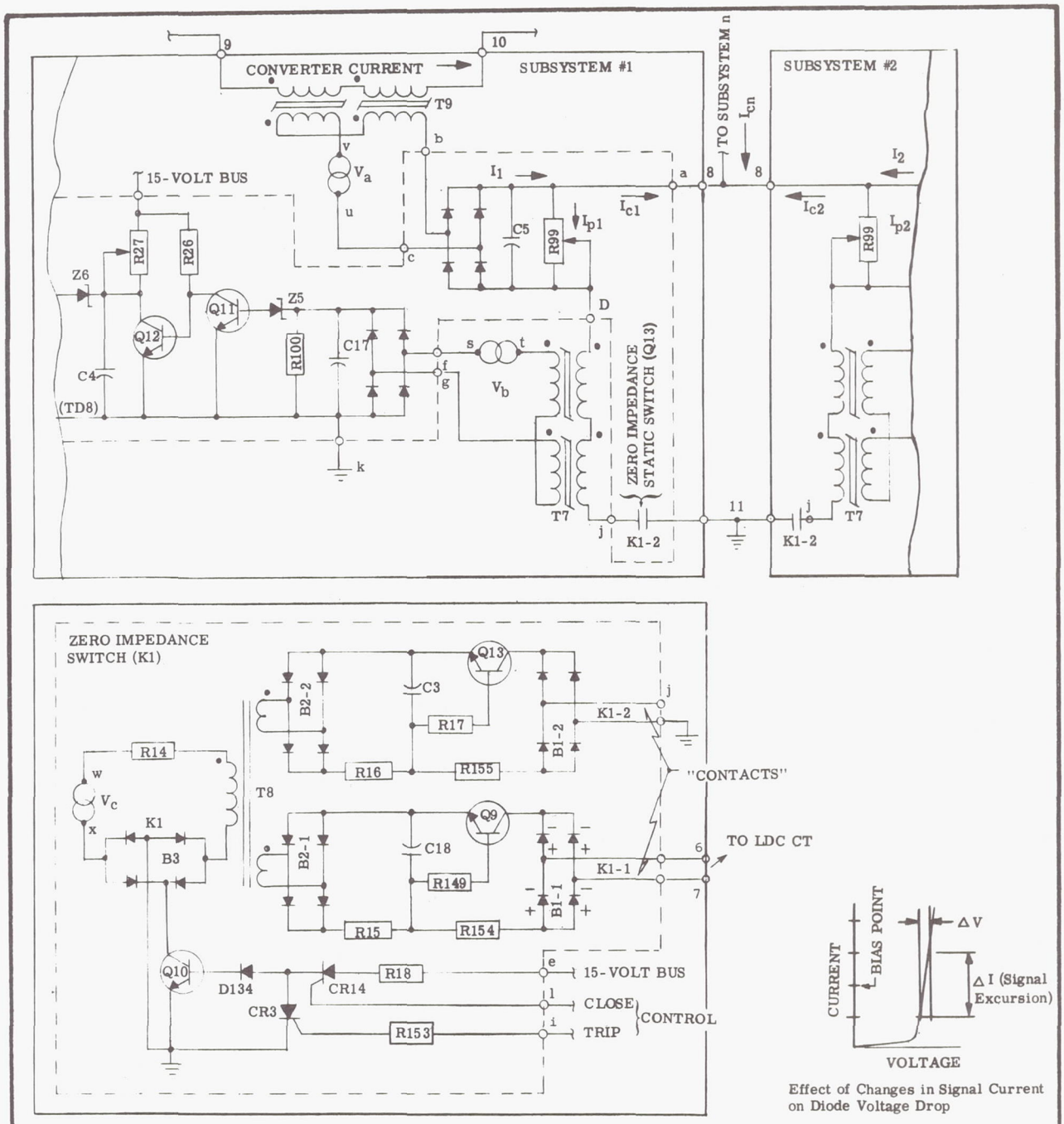
Load Division Protection

The function of the load division protection circuit is to determine when the unbalance current among the paralleled converters is greater than 15 percent of rated current. In order to accomplish this the magnitude of the difference current must be determined. Because the converters do not always operate in parallel, a control function must be included to prevent the load-division protection circuit from operating when a converter subsystem is not operating in parallel. The first of these requirements is provided by the transductor circuits T9 and T7 of figure 18. The second function is provided by a "switch" which prevents both the load-division protection and load-division control (located in the converter) from operating in an unparalleled converter. A description of each of these circuits follows.

Operational description of transductor control switch. - Since load-division control and protection circuits are required only when a subsystem is paralleled to the system tie bus, a means of controlling these circuits is required. The method chosen for the converter system is to disconnect one side of the output of the current sensor by effectively putting a "relay contact" in series with circulating current loop. When the "relay" is closed, the circuit is operative. Figure 23 shows a schematic of the load-division protection circuits for a two-converter parallel system including the "relay contacts".

An isolated, transistor, bi-laterial switch was chosen as the transductor control switch to avoid using a mechanical relay. However, a conventional transistor switch could not be used because the load-division control circuit required a very low series impedance. Therefore, the conventional circuit was modified to effectively provide zero impedance to the flow of signal currents in bridges B1-1 and B1-2 of figure 23. The static switch consists of two outputs (or contacts) K1-1 and K1-2. Both operations are identical. The static switch consists of three parts: the control, the isolated power supply, and the contacts. The control consists of controlled rectifiers CR3 and CR14, transistor Q10, and bridge B3.

The controlled rectifiers provide trip and close signals to Q10. The controlled rectifiers are latching or memory circuits. Isolation is provided by transformer T8. The ac voltage, V_C, is applied across the primary of T8 whenever Q10 and CR14 are on and CR3 is off. Now referring only the "contact" K1-2 the voltage of T8 is rectified by bridge B2-2 and filtered by R16 and C3. The output voltage of B2-2 turns on Q13 through R17. This allows current to flow through bridge B1-2, R155 and the collector of Q13. The diodes in B1-2, are therefore forward biased, and a voltage drop from anode to cathode is established. The signal current



Effect of Changes in Signal Current on Diode Voltage Drop

1. Reference Figure 18
2. V_a, V_b, & V_c Royer Oscillator Outputs
3. Switch CLOSE signal is from the DTB or the AP circuit
4. Switch TRIP signal is from the LBC-TRIP or the TBC-TRIP circuit

Figure 23. - Load-Division Sensing and Control Circuit

through "contact" K1-2 can therefore flow backward through a pair of diodes as long as the signal current is less than the bias current. Zero voltage drop is approached since the signal current flows through two diodes from cathode to anode (plus to minus) and through the other two diodes from cathode to anode (minus to plus). The curve on figure 23 shows the small change in diode voltage with the relatively large change in diode current. The drop across bridge B1-2 is reduced from 1.7 volts for the conventional switch to a maximum of 0.1 volts for the biased switch. Switch contact K1-1 operates in the same manner and is turned on or off at the same time.

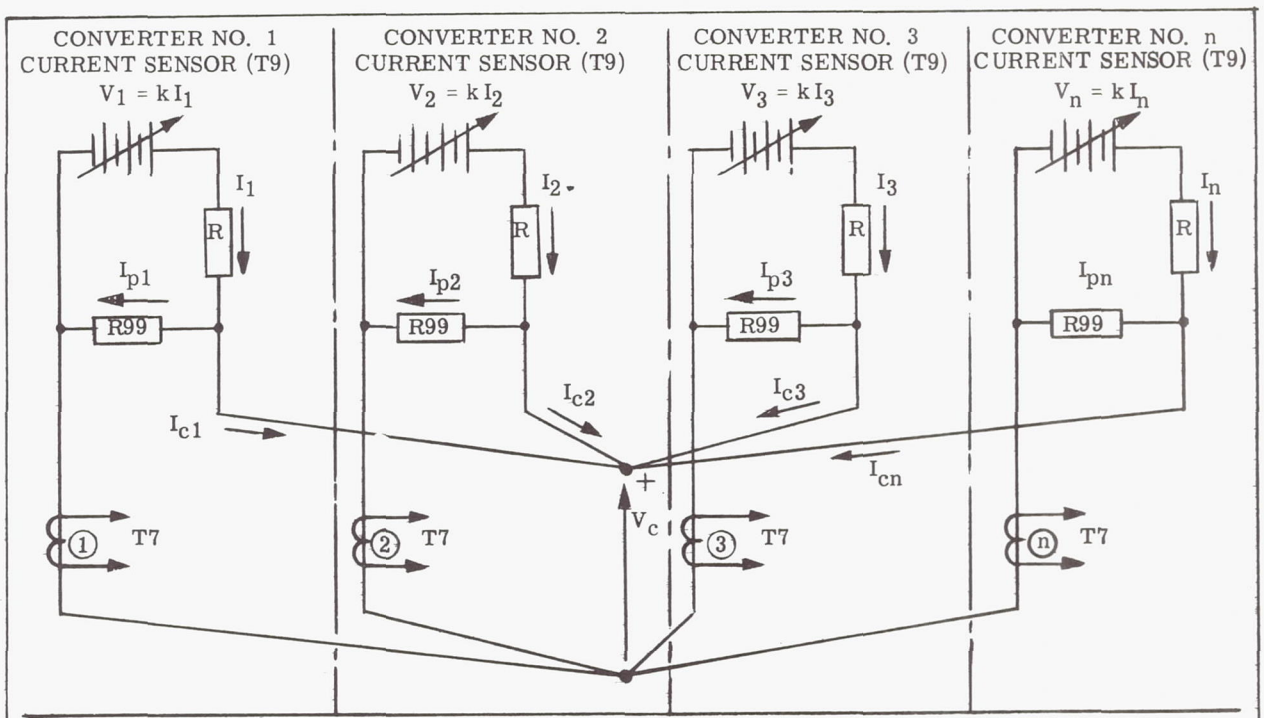
The switch is tripped by turning CR3 on. This shunts the close signal of CR18 to ground turning Q10 off. With Q10 off, transformer T8 is de-energized, and bridges B2-1 and B2-2 have zero output. Transistors Q9 and Q13 are turned off since their base currents are now zero. The bridge bias currents are therefore zero. Signals at K1-1 and K1-2 back bias two of the diodes in opposite legs according to the polarity of the signal voltage. The signal current is thus prevented from flowing through bridges B1-1 and B1-2, and the signal voltages are transferred to transistors Q9 and Q13. Since Q9 and Q13 have been turned off, no signal current can flow, and the switch "contacts" are open.

Operation of load-division sensing circuit. - Figure 23 reproduces the portion of figure 18 that senses the unbalance current between paralleled subsystems. The control windings of transductor T9 carry the converter load current. Figure 23 shows that R99 of each paralleled subsystem is connected in parallel. Therefore if the currents in each converter are equal, the voltages developed across R99 are equal and no circulating current flows ($I_{c1} = I_{c2} = 0$). However, if the converter currents are not equal, a circulating current must flow so that the voltage developed across pins 8 and 11 (ground) of each subsystem are equal. The following discussion will be limited to a two-converter parallel system. Extension to an n-converter parallel system is discussed in the next part of this section.

Potentiometers, R99, are adjusted to equal voltages for equal converter current. The circulating currents, I_{c1} and I_{c2}, will be equal but of opposite sign whenever an unbalance in converter currents exists. For example, if subsystem 1 has the larger output current, I_{c2} will equal minus I_{c1}. Assuming zero drop in the control windings of T7, the voltage from pin 11 to pin 8 is equal to R99 (I_1-I_{c1}) which is also equal to R99 (I_2+I_{c1}). The circulating current is therefore proportional to the difference in converter output current. The circulating current is measured by transductor T7. The voltage developed across R100 is therefore proportional to the current unbalance between converters. Since

this example is a two-converter parallel system, the voltages developed across R100 in each subsystem are equal. The trip point is determined by reference Zener diode, Z5. The load-division protection circuit provides an output whenever the current unbalance is in the range of 10 to 20 percent of rated current. When Zener diode Z5 breaks down, Q11 is turned on and Q12 turned off starting time delay TD8. If the current unbalance persists beyond TD8, Q59 is turned on and Q60 is turned off. A signal to pin H is thus provided to the TBC control circuit.

Circuit operation for three or more subsystems. - The load-division protection selected for this system does not provide selective tripping for a two-converter parallel system. However, if one of the two TBC's is tripped, the system is effectively isolated, and selective tripping for a two-converter is not necessarily required. To show how a faulted subsystem can be determined in an n-converter (n greater than 2) parallel system, the circuit of figure 24 is solved for the circulating current or fault signal.



NOTES:

1. All Load Current Sensors (Transductor T9) are Identical
2. All Resistors R are Identical
3. All Resistors R99 are Identical
4. Transductor T7 Senses Circulating Currents (I_{cn}), See Figure 23
5. Voltages V_1, V_2, V_3, $\cdots$, and V_n are proportional to Converter Output Current

Figure 24. - Simplified Load Division Sensing Loop

Assuming that the current sensors in each subsystem are identical and that all like circuit elements are identical, the simplified load-division sensing circuit of figure 24 can be solved to show the effect of a faulted converter in a parallel system consisting of n converters.

The load-division sensing circuits sense the circulating currents designated I_{cn} in figure 24 using transductor elements T7 of figure 23. The following development will determine the magnitude of the circulating circuit in terms of circuit constants, number of parallel systems, and the difference current between subsystems.

Assuming that only one converter is faulted at a time (say system No. 1), the currents in the other subsystems are equal. This means that

$$V_2 = V_3 = V_n$$

Summing the circulating currents

$$I_{c1} + I_{c2} + I_{c3} + \cdot \cdot \cdot + I_{cn} = 0 \qquad (22)$$

The circulating currents are

$$I_{c1} \triangleq I_1 - I_{p1}$$

$$I_{c2} = I_2 - I_{p2}$$

$$I_{c3} = I_3 - I_{p3}$$

$$I_{cn} = I_n - I_{pn}$$

The currents from the current sensors are

$$I_1 = (V_1 - V_c)/R \qquad (23)$$

$$I_2 = (V_2 - V_c)/R$$

$$I_3 = (V_3 - V_c)/R$$

$$I_n = (V_n - V_c)/R \qquad (24)$$

But

$$V_2 = V_3 = V_n$$

Therefore,

$$I_2 = I_3 = I_n \tag{25}$$

The currents in the shunt resistors (R99) are

$$I_{p1} = I_{p2} = I_{p3} = I_{pn} = V_c/(R99) = I_p \tag{26}$$

Equations (25) and (26) show that the circulating currents I_{c2}, I_{c3}, and I_{cn} are equal and equation (22) becomes

$$I_{c1} + (n-1)\ I_{cn} = 0 \tag{27}$$

Solving for V_c in equations (23) and (24)

$$V_c = V_1 - I_1 R = V_n - I_n R$$

and solving for I_n

$$I_n = I_1 + (V_n - V_1)/R \tag{28}$$

However,

$$I_1 = I_{c1} - I_p \text{ and } I_n = I_{cn} - I_p$$

Therefore, equation (28) reduces to

$$I_{cn} = I_{c1} + (V_n - V_1)/R \tag{29}$$

Substituting equations (29) into equation (28)

$$I_{c1} = -(n-1)(I_{c1}) - (n-1)(V_n - V_1)/R$$

which becomes

$$I_{c1} = \left(\frac{n-1}{n}\right)\left(\frac{V_1 - V_n}{R}\right) = \left(\frac{k(n-1)}{Rn}\right)(I_1 - I_n) \tag{30}$$

$$I_{cn} = -\left(\frac{1}{n}\right)\left(\frac{V_1 - V_n}{R}\right) = -\left(\frac{k}{Rn}\right)(I_1 - I_n) \tag{31}$$

The currents I_{c1}, I_{c2}, . . ., and I_{cn} are sensed by transductor elements T7 as described above. The output voltages of these circuits provide the TBC trip signals through time delay TD8.

Equations (30) and (31) show that the current in the faulted converter (I_{c1}) is always greater than the current in the unfaulted converters (I_{cn}). This situation provides the necessary criteria for selecting a faulted inverter from a parallel system consisting of three or more converters. When a parallel system consists of only two converters, the detection circuit will provide a fault signal to unparallel the converters, but the faulted converter may not be selected since I_{c1} is equal to I_{cn} for a two-converter system. Also, note that equations (30) and (31) above have the same form as equations (9) and (10) of the earlier description of "Load Division Protection." The selective tripping and trip sensitivity problems of the inverter load-division protection circuits are, therefore, the same for the converter load-division protection circuits. See the discussion of equations (9) and (10) for more detail.

Using this characteristic of the load-division circuit, a faulted converter in a parallel system consisting of three or more converters may be selected in one of two ways. The simplest is to apply the output of transductor T7 (voltage proportional to current unbalance) to an inverse time delay.

Since the faulted system always has the highest voltage, a properly selected inverse voltage-time characteristic will trip only the faulted system. The inverse time delay has the following requirements.

(1) The minimum time must be long enough to allow recovery from transients resulting from load switching, fault removal, or paralleling.

(2) The slope of the voltage time curve must be selected to provide enough time difference between subsystems to prevent overlap in contactor operation and transient recovery time of the unfaulted subsystems.

(3) The inverse time characteristic must be compatible with the current limiting circuits of the converter.

(4) The time characteristic must take into consideration the overcurrent protection and the overvoltage protection circuits if inverse time delays are used.

(5) The minimum trip point (amount of unbalance allowed with no trip) must be compatible with the inverter load-division control circuit.

Figure 25 shows a typical circuit using the inverse time delay approach to selective tripping.

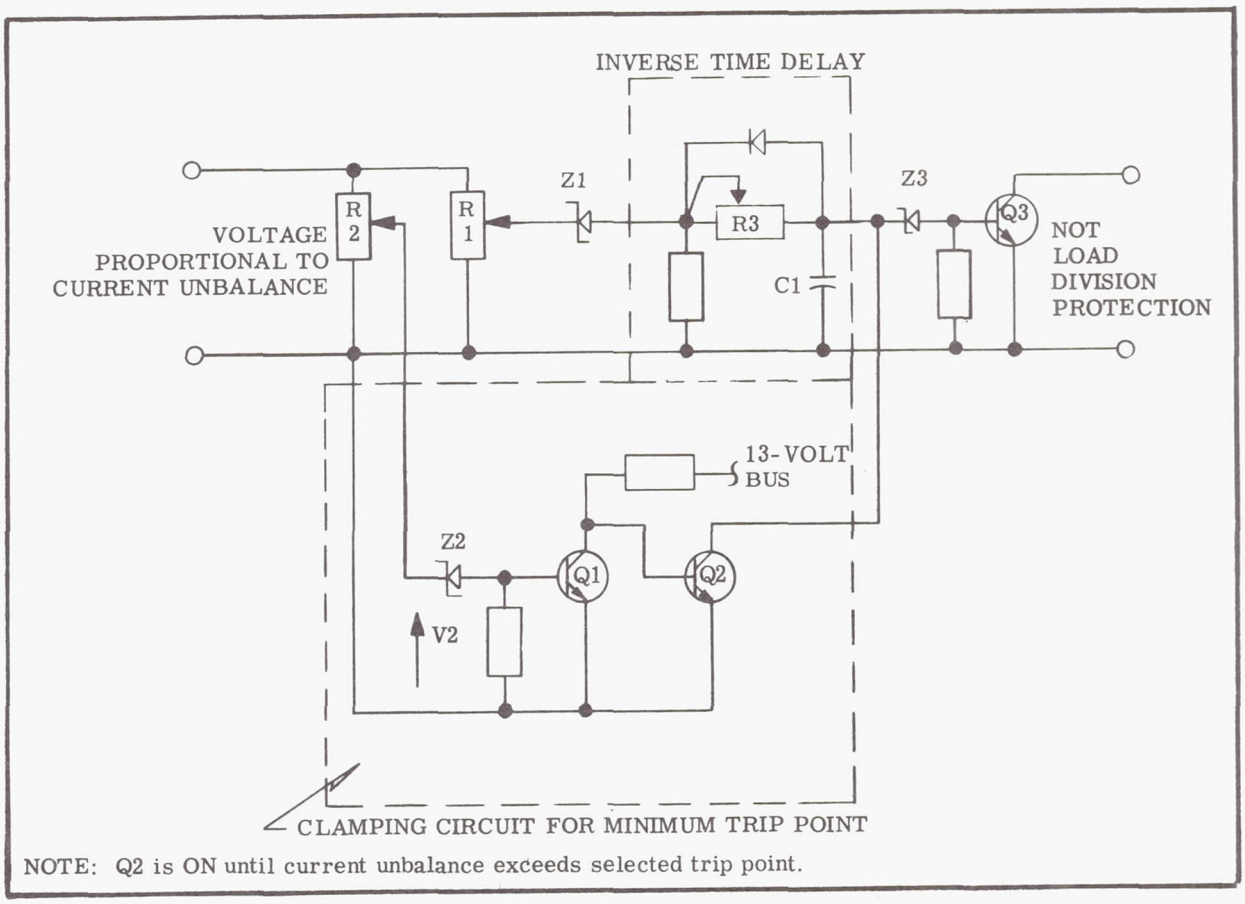


Figure 25. - Load Division Fault Selectivity Circuit in an n-Subsystem Parallel System

Another approach to selective tripping is shown in figure 26. This circuit effectively compares the voltage developed across each sensing circuit to the voltage developed by the faulted subsystem. The output of this circuit may be applied to either a fixed or an inverse time delay. This approach, while requiring slightly more complex circuits, is not affected by considerations (2), (3), and (5) and considerations (1) and (4) are greatly simplified since the time delay is independent of the fault selectivity requirements.

The operation of the circuit centers around the voltage comparator WS304 of figure 26. A reference voltage is applied to pin 8. The reference chosen is from the cathodes of diode D1 in all control and protection circuits. Since the faulted system always has the highest voltage (n greater than 2), diode D1 in all other subsystems will be back biased; therefore, the voltage

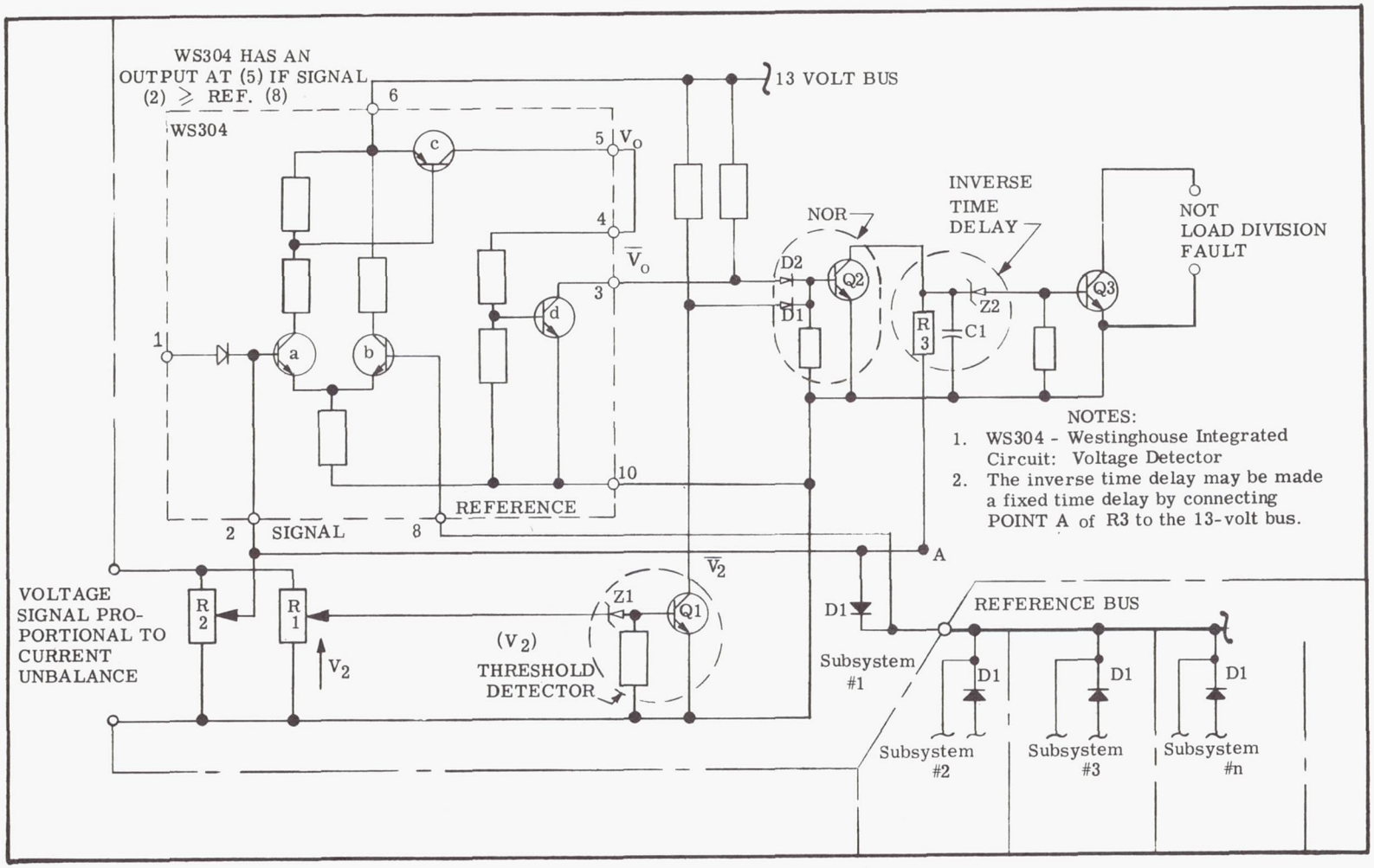


Figure 26. - Comparator Circuit for Load-Division Fault Selectivity in an n-Subsystem, Parallel System (N ≥ 3)

on the reference bus will be that of the faulted system. Pin 2 of WS304 is connected to the anode side of D1 or the actual output of each load-division sensing circuit. Pin 5 will have no output ($V_o = 0$) so long as the voltage at pin 2 is less than the voltage at pin 8. However, if pin 2 is equal to or greater than pin 8, transistor (a) turns on; this turns transistor (c) on and 13 volts is available at pin 5. Since the reference voltage and the comparison voltage are equal only on the faulted subsystem, only the comparator in the faulted subsystem will have an output. The voltage drop across diode D1 ensures a slightly positive voltage difference from pin 2 to pin 8. This comparator circuit typically operates at about 0.05 volts differential. Since this circuit can have an output under normal operating conditions, a threshold detector is used to provide an output only when the load-division error is in the range of 10 to 20 percent. Zener diode Z1 provides this function. The time delay is started only when both the threshold (V_2) is reached, and the voltage comparator has an output V_0 or start time delay (T) when $V_0 \cdot V_2$. This can be modified to

$$T = V_0 \cdot V_2 = \overline{\overline{V}_0 + \overline{V}_2}.$$

Transistor (d) in WS304 and transistor Q1 provide the NOT V_0 and NOT V_2 functions. Diodes D2 and D3 provide the OR function and transistor Q2 provides the third NOT function. This means that Q2 is off only when both V_0 and V_2 are present. The time delay may be either fixed or inverse by connecting R3 either to the 13-volt bus or to the arm of potentiometer R2, respectively. Transistor Q3 turns on whenever the voltage across C1 exceeds the Zener diode voltage of Z2. The output of this circuit is zero when a load-division error exceeds 10 to 20 percent of rated current on a faulted subsystem.

RELIABILITY ANALYSIS

The analysis presented herein defines the estimated failure rate of a single-converter or single-inverter control and protection circuit. This failure rate, in conjunction with the failure rate of other subsystem components, determines the reliability of a parallel electric power system. To estimate the reliability of the control and protection circuits, the following criteria were established.

(1) Only steady-state operating conditions were considered for each component.

(2) Operation only at 25°C ambient temperature was considered.

(3) The reliability estimate was based on using high reliability components. The failure rates for most of the components were obtained from information available on the Apollo reliability program. In cases where this information was not available, MIL-HDBK-217 was used.

(4) All components were considered equal on the assumption that failure of a part would cause malfunction or failure of one or more of the automatic control and protection circuits.

(5) Only nominal component values were used for electrical stress levels. Maximum variations in tolerances were not considered.

(6) The following parameters were considered most critical for each component.

Capacitors - Working Voltage
Controlled Rectifiers - Junction Temperature
Diodes - Peak Inverse Voltage and Junction Temperature
Resistors - Power Dissipation
Transistors - Junction Temperature
Transformers, Chokes, Transductor Elements - Power Dissipation (Hot-Spot Temperature)
Zener Diodes - Junction Temperature

(7) The stress level of critical parameter on all components is 50 percent of the rated value. Because all transistors operate in the switching mode and the power supply characteristics are known, there are no critical components or parameters in the C/P circuits.

(8) All adjustable resistors were replaced by two fixed resistors. This increases reliability by using components with a lower failure rate.

With these ground rules, and the failure rates specified in table VI, the composite failure rate was established. The failure rate and number of components are listed in table VII for the inverter and in table VIII for the converter.

Since neither a detailed failure-mode analysis was required nor a mission defined, the actual effect of the control and protection circuits on subsystem reliability cannot be established. The failure rates estimated in tables VII and VIII, however, present a worst-case condition, i.e., any failure within the C/P circuits is considered to fail the entire subsystem. In the actual case, however, many C/P circuit failures would not cause a subsystem to false trip but would simply cause a loss of a protective function.

Table VI. - Failure Rates and Stress Level of Components Used in Control and Protection Circuits

COMPONENT	FAILURE RATE %/1000 hours	BASES OF FAILURE RATE
Capacitors (Solid Tantalum)	0.0005	Operating at 50% rated working voltage at 40°C ambient. Supplier: Kemet Corp. Supplier calculation based on 5.2 million unit hours at maximum rated voltage and temperature.
Controlled rectifier (Power)	0.06	Junction temperature of 60°C in 25°C ambient temperature. One operation every 50 hours for maximum of 20 milliseconds. 2N2027 Type tested to proposed Mil spec with added screening tests. Minuteman part failure rate used because part is manufactured by the same process used in minuteman parts. Supplier: General Electric
Controlled rectifier (Small signal)	0.01	Mil part with additional screening tests. Minuteman part failure rate used because part is manufactured by the same process used in minuteman parts. Junction Temperature of 60°C in 25°C ambient. Supplier: Solid State Products
Diode	0.0001	Based on 60°C junction temperature at 25°C ambient. Supplier: General Electric Part is manufactured from the Minuteman production line with additional screening tests.
Resistors	0.0001	Based on operating at 50% of rated power at 25°C ambient.
Transistors	0.01	Based on junction temperature of 60°C in 25°C ambient. Supplier: RCA Basically a 2N2102 type transistor with additional testing. Failure rate is from Minuteman med. power transistor.
Transductor Elements, Chokes, Transformers	0.050	Based on maximum hot-spot temperature of 50°C at 25°C ambient and MIL-HDBK-217. Supplier: WAED, Lima, Ohio
Zener Diode (Small signal)	0.005	Based on junction temperature of 60°C in 25°C ambient temperature. Mil part with added screening tests.
Zener Diode (Power) and Power Diodes	0.12	Based on junction temperature of 61°C in 25°C ambient temperature. Mil part with added screening tests Supplier: Motorola
Resistor (Power)	0.110	Operated at 50% of rated power in ambient of 25°C.

Table VII. - Calculation of MTBF for Inverter Control and Protection Circuits

COMPONENT	NUMBER OF COMPONENTS (n)	FAILURE RATE (λ, %/1000 hours)	TOTAL COMPONENT FAILURE RATE ($n\lambda$)
Capacitor	44	0.0005	0.022
Controlled Rectifier (Power)	2	0.06	0.12
Controlled Rectifier (Small Signal)	0	0.01	0.0
Diode (Small Signal)	103	0.0001	0.0103
Diode (Power)	0	0.12	0.0
Resistor (Small Signal)	169	0.0001	0.0169
Resistor (Power)	3	0.110	0.33
Transistor (Small Signal)	58	0.01	0.58
Chokes and Transformers	16	0.05	0.80
Zener Diode (Small Signal)	25	0.005	0.125
Zener Diode (Power)	1	0.12	0.12
		Total (λ_t)	
		MTBF = $10^5/\lambda_t$ = 47,081	

Table VIII. - Calculation of MTBF for Converter Control and Protection Circuits

COMPONENT	NUMBER OF COMPONENTS (n)	FAILURE RATE (λ, %/1000 hours)	TOTAL COMPONENT FAILURE RATE ($n\lambda$)
Capacitor	26	0.0005	0.013
Controlled Rectifier (Power)	6	0.06	0.36
Controlled Rectifier (Small Signal)	8	0.01	0.08
Diode (Small Signal)	100	0.0001	0.01
Diode (Power)	1	0.12	0.12
Resistors (Small Signal)	139	0.0001	0.0139
Resistors (Power)	1	0.110	0.110
Transistors (Small Signal)	47	0.01	0.47
Transductor Elements or Transformers	14	0.05	0.7
Zener Diode (Small Signal)	18	0.005	0.09
Zener Diode (Power)	1	0.12	0.12
		Total (λ_t)	
	MTBF = $10^5/\lambda_t$ = 47,900		

A complete analysis would separate those failures resulting in a false trip of a portion of a subsystem from those failures resulting in loss of a protective function. The reliability of the C/P circuits would therefore be:

λ_f = failure rate of components that result in a false trip of the C/P circuit

λ_{1n} = failure rate of components that result in loss of given protective function

t = mission time

P_{fn} = probability of a given fault occurring

n = n^{th} protective function

$R_f = EXP[-\lambda_f t]$

$R_{1n} = 1 - (1 - EXP[-\lambda_{1n} t]) \cdot P_{fn}$

The C/P circuit reliability is then

$$R_{C/P} = R_f \cdot R_{1_1} \cdot R_{1_2} \cdots R_{1n}$$

If the probability of a fault is considered to be 100 per cent, then the circuit reliability is simply

$$R_{C/P} = EXP[-(\lambda_f + \lambda_{1_1} + \ldots + \lambda_{1n})t].$$

For a subsystem consisting only of the inverter or converter and the associated control and protection circuits the subsystem reliability is simply the product of the reliabilities of the C/P circuits and the inverter or converter. A reliability model would have to be generated for more complex subsystems.

Obviously, if no failures within a subsystem can be tolerated, the addition of C/P circuits would only decrease the chance of success. However, if more system capacity is provided than is required, portions of the parallel system may be lost and still meet mission requirements. This, in effect, increases system reliability through parallel redundancy. Further, if mission success, in terms of available electric power, can be met by multiple levels of required power, the C/P circuits will add materially to the attainment of a successful mission by removing faulty portions of the power system.

SYSTEM TESTS

To demonstrate the operation of the automatic control and protection circuits, tests were run on a two-inverter parallel system and a two-converter parallel system. These system tests were divided into three parts: manual, isolated, and parallel.

Sample oscillograms are provided for each test condition to illustrate system operation. These traces also show transient response and sequencing of the protective functions to isolate the fault.

Results and Analysis of Parallel Inverter System Tests

Manual system operation. - The tests during manual system operation showed that each inverter can be operated manually, exclusive of all automatic control and protection. Further, these tests demonstrated that the basic performance of a parallel inverter system is unaffected by the addition of the automatic control and protection circuit.

Before the test was initiated, all the contactors in the system were tripped and the dc power supplied to the system was adjusted to 28 volts. Both manual override switches were placed in the MANual position. Subsystem No. 1 was tested first followed by subsystem No. 2.

A futile attempt to start the inverter automatically by closing the inverter control switch demonstrated that automatic start-up is locked out when the manual override switch is in the MANual position. The inverter control switch was placed back in the TRIP position and the ICC manual switch was momentarily closed to start the system manually. The system started and built up to an output voltage of 115 volts, ac, rms per phase after approximately 5 seconds.

The load bus contactor was closed manually by momentarily placing the LBC manual switch in the CLOSE position. This connected the load to the inverter. The load was then adjusted to rated value (2.18 amperes per phase). The output voltage remained at 115 volts demonstrating that the inverter voltage-regulating circuit was operating properly. Then the inverter was manually connected to the system tie bus by momentarily placing the TBC manual switch in the CLOSE position. Several faults were placed on this subsystem to demonstrate that fault protection is not provided when the inverter is manually operated. The inverter output was increased to about 125 volts and then decreased to about 95 volts with no resulting trips. The line connecting the

inverter 3200-Hz terminals was then shorted to ground, thus eliminating the 3200-Hz tuning fork reference signal from the input to the inverter unijunction oscillator. This made the inverter free-running at its unijunction oscillator natural frequency, which at this time was 360 Hz. Since no trip occurred when the 3200-Hz line was shorted, this test showed that the abnormal frequency protection circuit was locked out as desired. The short was then removed from the 3200-Hz line.

A short was next placed from phase A of the inverter and output to ground and then removed. This simulated a differential current fault and did not cause a trip. A short at the load was placed across phase A to ground simulating a load bus fault. This also caused no trip. The short was removed.

The second inverter was started and connected to its load in the manner described above. Figure 27 shows the phase relationship of phase A of each inverter before and after locking the inverter clocks into phase. The inverter, having been locked into phase, the TBC of subsystem No. 2 was closed. Table IX shows the data for isolated and parallel system operation. Columns 5 and 6 of table IX show that the inverters were properly sharing load.

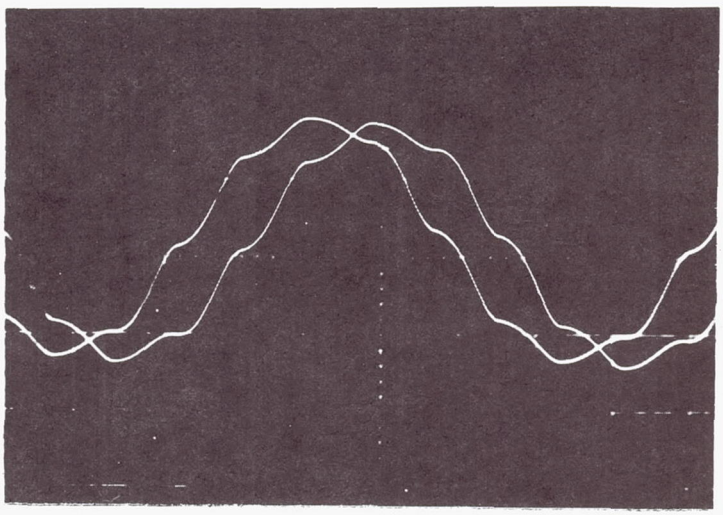
The tie bus was shorted from phase A to ground. No trips occurred, showing that the overcurrent protection circuits are not operative during manual operation. The tie bus short was removed.

Continuity on the tie bus was then broken by opening the tie-bus switch. This separated the two subsystems while their tie-bus contactors remained closed. The load was removed from inverter No. 2 by opening its manual load removal switch. This simulated a severe load unbalance condition. No trip occurred showing that the load-division protection circuits are inoperative during manual operation. The tie-bus switch was then closed and the load placed back on inverter No. 2.

These tests demonstrate conclusively that manual operation of the inverter system is not affected by the control and protection circuits.

Automatic, isolated system tests. - The purpose of this series of tests was to show the automatic operation of a single subsystem under normal and abnormal operating conditions. The "Inverter Control and Protection" section of this report describes how the system should operate.

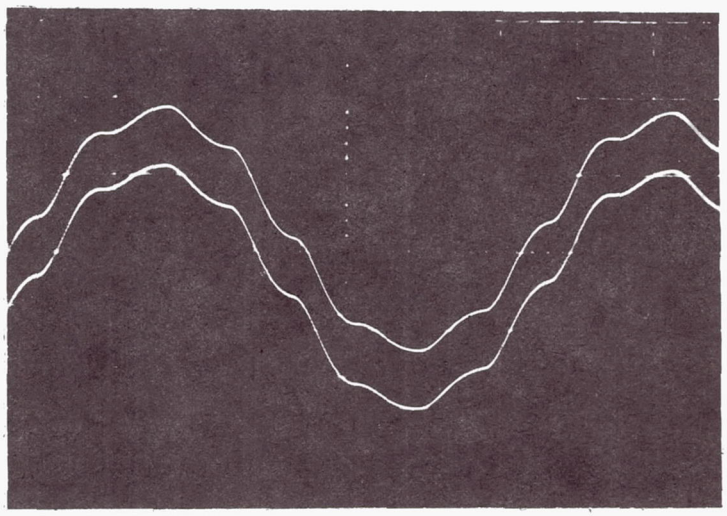
Automatic system startup and effect of manual control: This test demonstrates that the manual switches exercise no control over the system when the manual override switch is in the AUTOmatic position.



Phase A of Inverter No. 1

Phase A of Inverter No. 2

Shows Phase Relationship of Inverters before Inverter Clocks were Locked into Phase (Before closing S7)



Upper Trace:
Phase A of Inverter No. 1

Lower Trace:
Phase A of Inverter No. 2

Shows Phase Relationship of Inverters after Inverter Clocks were Locked in Phase (After closing S7)

Figure 27. - Manual Paralleling of Inverters

Table IX. - Test Results of Parallel Inverter System During Manual Operation

Condition	A		B		C	
System No.	(1) Isolated	(2) Isolated	(1) Isolated	(2) Isolated	(1) Paralleled	(2) Paralleled
Line-to-Neutral Voltage (volts)						
Phase A	115.4	114.9	116.5	115.0	114.2	114.2
Phase B	114.8	113.5	115.8	114.3	114.0	114.0
Phase C	115.2	113.0	116.3	115.5	115.5	115.0
Line Current (amps)						
Phase A	0	0	2	2	1.78	1.93
Phase B	0	0	2	2	1.75	1.95
Phase C	0	0	2	2	1.72	2.01
Power (watts)						
Phase A	0	0	231	227	202	220
Phase B	0	0	233	229	204	226
Phase C	0	0	235	230	198	230
Frequency (Hz)	400	400	400	400	400	400
Input Voltage (volts)	28.9	28.8	28	28	27.0	27.5
Input Current (amps)	3.8	3.5	35.8	34.7	41.1	36.8
Test Record	K1966949	K1966949	K1966949	K1966949	K1966956	K1966956

First, all contactors were placed in the TRIP position and both manual override switches were placed in the AUTO position. An attempt was made to start each subsystem and to close its contactors by operating the ICC, LBC, and TBC manual control switches. The contactors would not operate.

Each inverter was started by placing its inverter control switch (ICS) in the CLOSE position. The inverter reached a power ready condition and the load-bus and tie-bus contactors closed automatically. Each manual control switch was placed in the TRIP position, but the contactors still would not operate. The inverter was shut down by placing the ICS in the TRIP position. All contactors were immediately tripped.

These tests show that all manual controls are inoperative when the manual override switch is in the AUTOmatic position whether the inverters are operating or not.

Automatic systems startup, no-power-ready condition: This test demonstrates that an inverter will not automatically complete the startup sequence should one of the power-ready conditions not

be met. The power-ready conditions are that the phase voltage and frequency must be within the range listed in table X.

Table X. - Measured Trip Points of Inverter Automatic Protection Circuits

CIRCUIT		RANGE		MEASURED	
		Lower Limit	Upper Limit	C/P #1	C/P #2
Overvoltage	(OV), volts	120	126	121.3	120.1
Undervoltage	(UV), volts	102	108	104.1	105.3
Overfrequency	(OF), Hz	404	410	408	407
Underfrequency	(UF), Hz	390	396	393	393
Differential Current	(DP), amps	0.87	1.3	1.02	1.05
Load-Bus Overcurrent	(LOAD OCP), amps	2.51	2.73	2.65	2.7
Inverter Overcurrent	(INV OCP), amps	2.51	2.73	2.7	2.7
Load Division Protection	(LDP), amps	0.22	0.44	0.4	0.4
Time Delays (Seconds)					
TD1		10.8	13.2	13.1	10.8
TD2		0.99	1.21	1.2	1.16
TD3		0.47	0.58	0.52	0.54
TD4		0.34	0.41	0.38	0.39
TD5		0.20	0.25	0.24	0.24
TD6		0.61	0.74	--	--
TD7		1.26	1.54	1.5	1.3

Under an automatic startup condition, the inverter is started by closing the inverter control contactor (ICC). The inverter output remains at zero for about five seconds. At the end of this time delay, the output voltage will rise to a given value. If the power quality is proper, the LBC will close, stopping the no-power-ready time delay and ultimately closing the TBC. However, if the power quality is outside the limits given above, the LBC should not close, the ICC should trip, and the TBC should close after the no-power-ready time delay times out.

Table X lists the trip points for the four power quality fault sensors of subsystems 1 and 2. An undervoltage fault illustrates a typical no-power-ready condition for subsystem 1 and is shown in figure 28. The upper traces of figure 28 show the condition of the contactors. Note that the ICC and LBC have a common trip line. Closure of the ICC is indicated by a trace above the trip line (end of arrow) and closure of the LBC is indicated by a trace below the trip line (end of arrow). The trip line for the TBC is shown and closure of the TBC is indicated by a trace below the trip line (end of arrow). The next trace shows phase C of the inverter voltage.

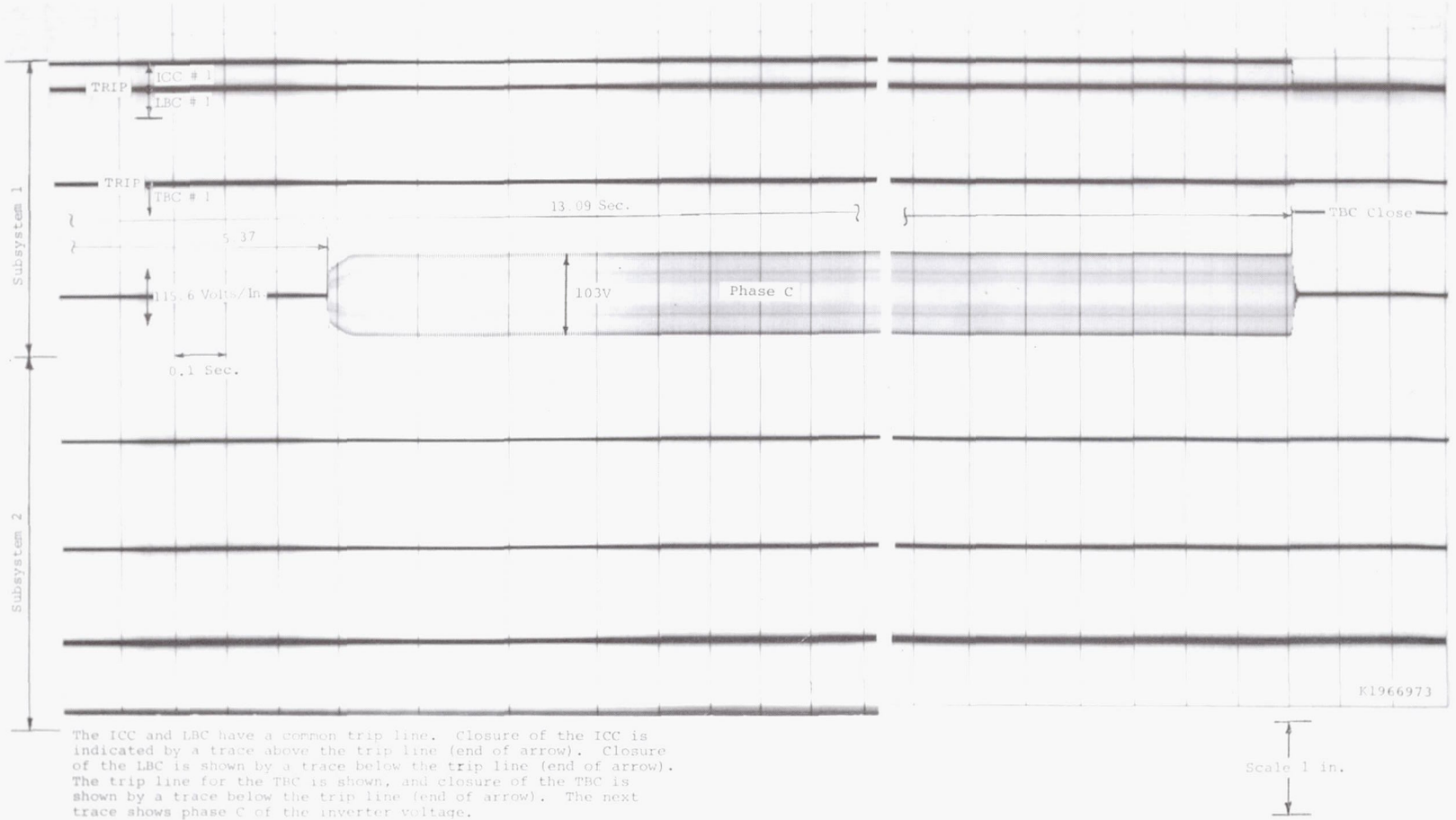


Figure 28. - No-Power-Ready Time Delay Test of Inverter No. 1 With an Undervoltage Condition

At the left edge of the traces, the ICC is shown closed and the LBC and TBC are shown tripped. The closure of the ICC is not shown because of the length of the trace. After 5.37 seconds the voltage builds up, but the LBC does not close because the terminal voltage is only 103 volts rather than the required 115 volts. The result of this condition is that the inverter continues to operate, isolated from all loads, until the no-power-ready time delay times out. This is indicated by tripping the ICC at the end of 13.09 seconds. Note that the terminal voltage is zero, the ICC and LBC are both tripped, and the TBC is closed at this point. This is the proper state of the subsystem containing an inverter which does not provide the proper quality of power.

The above tests show that the no-power-ready portion of the C/P circuits operated properly.

Power quality fault during single subsystem operation: This test demonstrates that the abnormal-voltage and abnormal-frequency protection circuits provide protection for inverter faults occurring during isolated subsytem operation. The OV, UV, OF, and UF sensing circuits provide signals to a 1.2-second time delay (TD2), which trips the ICC and LBC contactors and provides a close signal to the TBC. TD2 is also called the power-ready time delay. The sensors for abnormal voltage and abnormal frequency are the same as for a no-power-ready condition. The operating point of each sensor is listed in table X. As a means of illustrating the operation of subsystem, the consequence of an overvoltage fault on subsystem 2 is shown in figure 29.

The traces in figure 29 are the same as described in "Automatic systems startup, no-power-ready condition" above except the waveforms are for subsystem 2 rather than subsystem 1. At the left of the traces the subsystem is operating normally and all three contactors are closed. An overvoltage fault is applied as is indicated by the rise in voltage on phase C. After 1.2 seconds, both the ICC and LBC trip isolating the load bus from the inverter. The TBC remains closed so that the load bus may be supplied power from other inverters should one be connected to the system. The subsystems operate in an equivalent manner for the other power quality faults.

The above tests show that a power quality fault on a single subsystem properly isolates the faulted inverter and allows the load bus to be fed from other inverters through the tie-bus contactor.

Differential current protection for single subsystem (Zone 1): This test demonstrates the protection for a Zone 1 (see figure 1) fault. The differential current protection circuit operates immediately to trip the ICC and the LBC. There are eleven possible

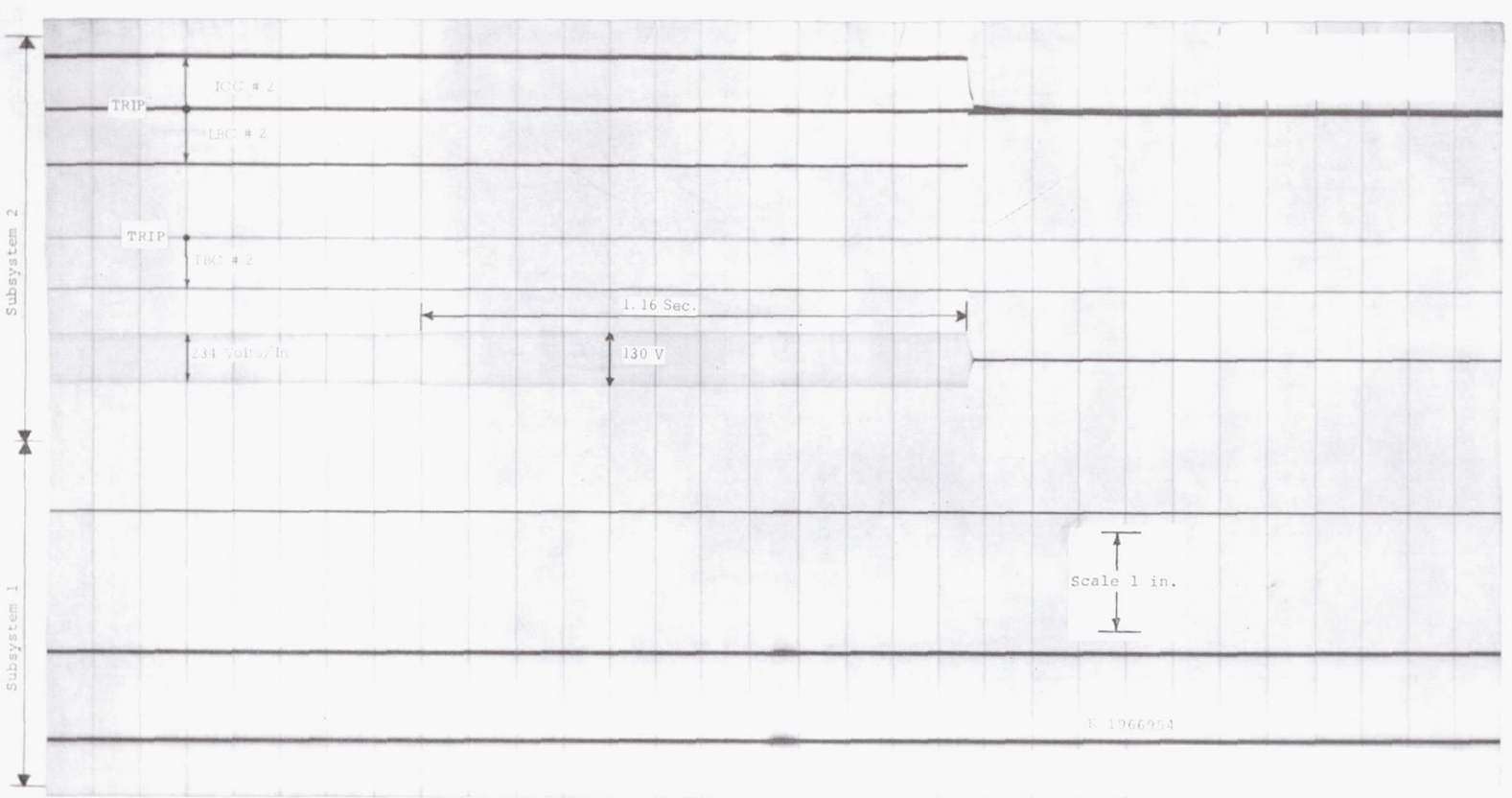


Figure 29. - Power-Quality Fault During Isolated Operation on Inverter No. 2

overcurrent faults for a three-phase, grounded neutral system. Figure 30 shows an oscillogram of a phase C-to-ground fault. Table X lists the calibration of the DP sensing circuits.

Figure 30 shows the result of a phase C-to-ground fault in Zone 1 of subsystem 1. The traces marked LBC, ICC, and TBC show the state of the contactors. The LBC and TBC are closed when a trace appears above the trip line and the ICC is closed when a trace appears below the trip line. These conditions are indicated by the arrow on each trace. The trace marked phase C is the current in phase C of the inverter. The DP fault is applied at a no-load condition and is indicated by the sudden rise in current. The fault, in this case, lasts for 0.007 seconds before the ICC and LBC trip.

This test shows that the differential current protection circuits provide the required operation for faults on a single subsystem.

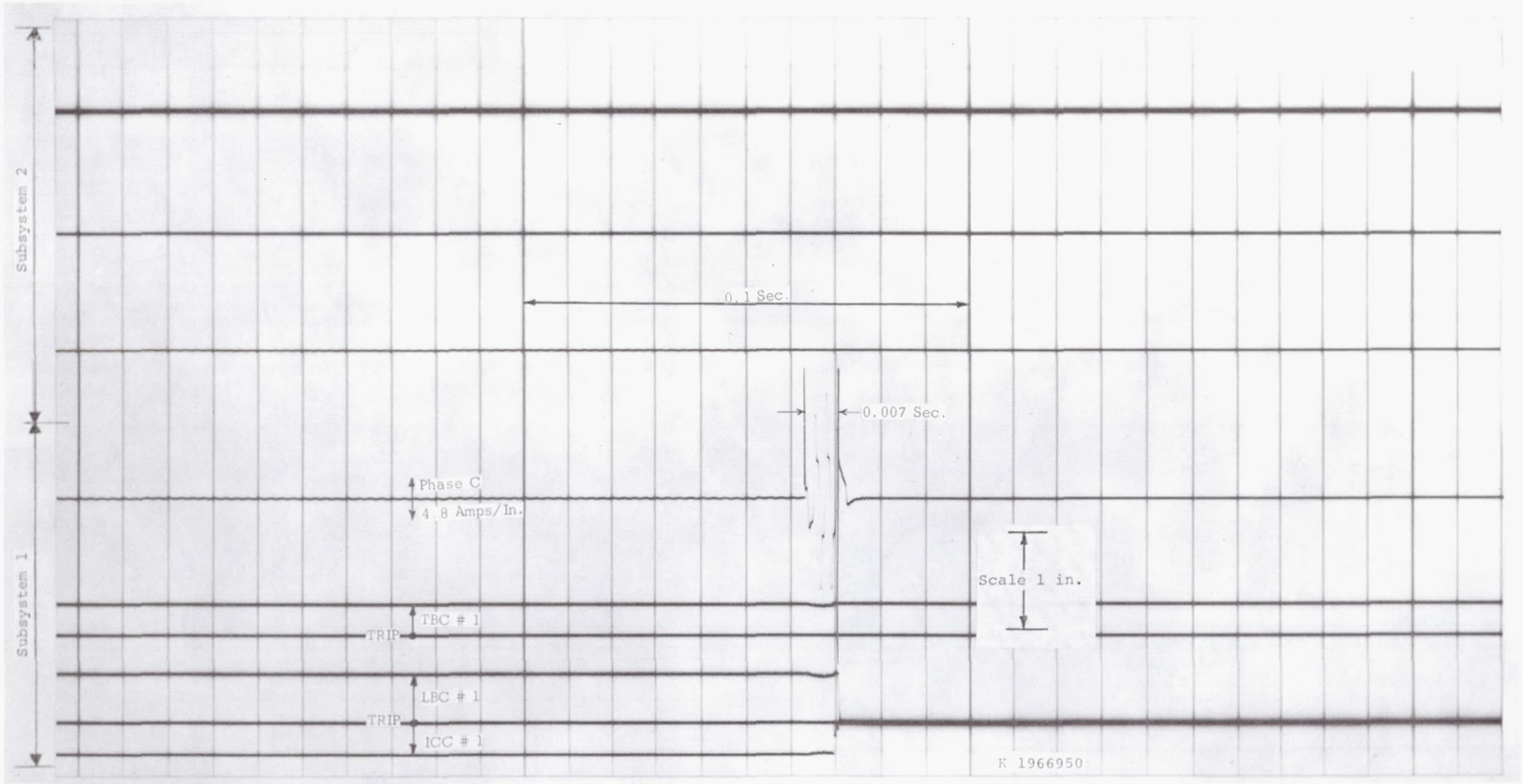
Automatic, parallel system operation. - The purpose of this series of tests was to show the automatic operation of a parallel inverter system under normal and abnormal operating conditions. The "Inverter Control and Protection" section of this report describes how the system should operate.

Automatic paralleling: As discussed in earlier sections, the purpose of the automatic paralleling (AP) circuit is to provide a means for bringing an inverter into phase with the parallel system without introducing frequency transients into the parallel system.

To achieve the objective of forcing an on-coming inverter into phase with a parallel system required the derivation of a blanking signal suitable for forcing an inverter into phase and then reverting back to the original blanking signal (BS) after paralleling had been completed.

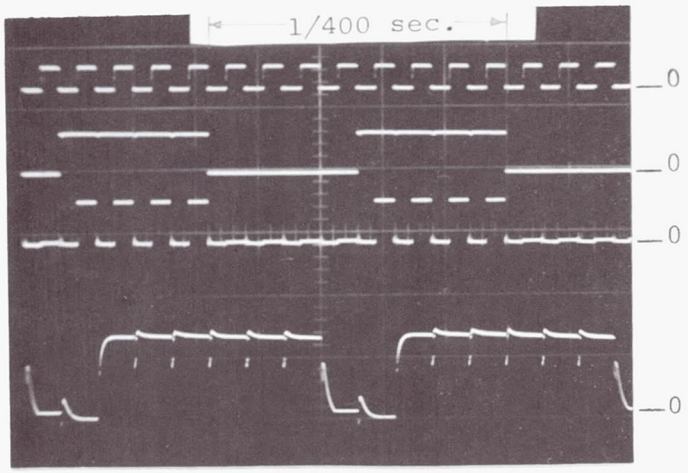
The following oscillograms show the various signals which were derived theoretically in the "Inverter Control and Protection Circuit Design" section and are shown in figure 15. Additional oscillograms show the operation of the auto-synchronizer from the startup of the initial system through the paralleling of a second system.

The derived waveforms of α and β which were presented in figure 15 were obtained experimentally and are shown in figure 31. Trace 1 of each picture is the output of the 3200-Hz reference oscillator. This is test point (TP) 5 of figure 14. Trace 2 of each picture is the state of transistor 18 and is TP 2 of figure 14. Trace 4 of each picture is the blanking signal generated by



The LBC and TBC are closed when a trace appears above the trip line; the ICC is closed when a trace appears below the trip line as shown by arrows.

Figure 30. - Inverter No. 1 - Isolated Phase C to Ground Fault on Inverter Feeder No. 1



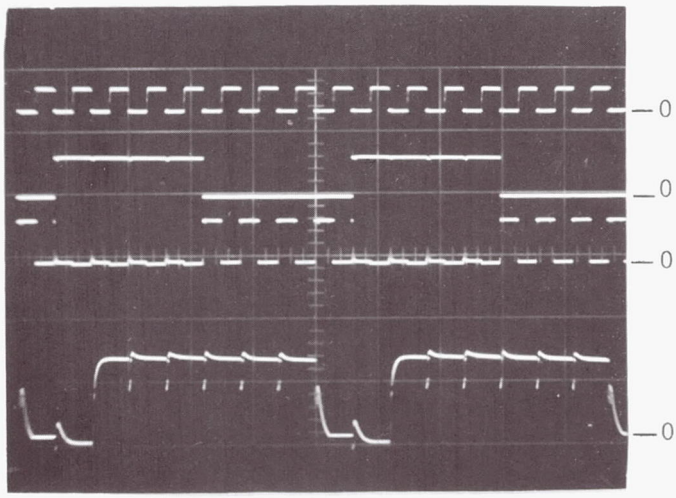
$\overline{R}$, (10V/Div.)

Q18A, (TP 2) 50V/Div.)

β, (TP 13) (2V/Div.)

BS, (TP X) (10V/Div.)

Generation of β



$\overline{R}$, (10V/Div.)

Q18A, ($\overline{A}$) (TP 2) (50V/Div.)

α, (TP 12) (2V/Div.)

BS, (TP X) (10V/Div.)

Generation of α

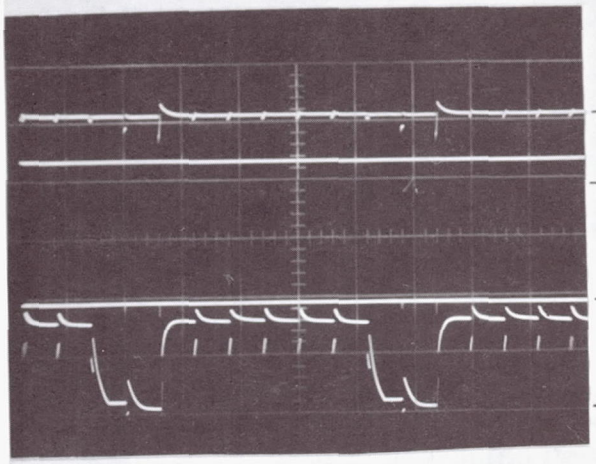
(TP refers to test points shown in Figure 14)

Figure 31. - Derivation of α and β for Auto-Sync Control

the inverter and is designated TP 3 or TP 10 depending on the point in startup cycle. Trace 3 of the upper picture is β (TP 6) which is generated by $\overline{A}$ and $\overline{R}$. Note that a one is generated only when both Q18A and $\overline{R}$ are one. Comparing trace 3 and 4 of the upper picture shows that adding β to the blanking signal through an OR gate will extend the leading edge of the blanking signal. Trace 3 of the lower picture is α (TP 12) which is generated by A and RO. Note that α is generated only when both Q18A and $\overline{R}$ are zero. Comparing traces 3 and 4 of the lower pictures shows that α will extend the trailing edge of the blanking signal when these two signals are added through an OR gate. Close inspection of trace 3 shows that a narrow pulse is generated at the point where Q2A changes state. This was predicted in the theoretical derivation of α. This narrow pulse would normally interfere with the switching of Q18A and is the reason for eliminating the SUSS after the inverter has been paralleled. The SUSS is effectively an open-loop design and, therefore, this narrow pulse is eliminated by the normal delay of Q24 of figure 6 turning off. The following oscillograms will confirm this.

The next two sets of oscillograms describe the operation of the inverters under two modes of startup. The first mode, shown in figure 32, describes the operation of the synchronizer for the first inverter being connected to a parallel system. Under this condition, the two sync busses must have the proper signals applied to them because the only signal of value at this time is the internal blanking signal of the inverter. Referring to figure 14, the signals of the OR, in the synchronizer, must be zero to ensure proper inverter startup because an external one signal will stop the inverter. In order to ensure zeros to the OR gate, the sync bus must have a zero signal while the SUSS bus must have a one signal. Traces 1 and 2 of the upper picture of figure 32 confirm that the two busses have the proper signals. Trace 3 of this picture shows that the SUSS gating transistor inverts the one of the SUSS bus such that the required zero is applied to the OR gate.

The lower picture of figure 32 shows the state of the synchronizer after inverter No. 1 has been paralleled to the tie bus (TBC closed). Each trace of the lower picture is taken from the same test points (figure 14) employed in the upper picture. In the lower picture, the first trace shows a sync signal on the sync bus in phase with the blanking signal (BS). The second trace shows a signal on the SUSS bus. The third trace shows that the SUSS is not being injected into the blanking signal. The lower picture, therefore, shows that the logic circuits work properly for the startup of the initial inverter in a parallel system.



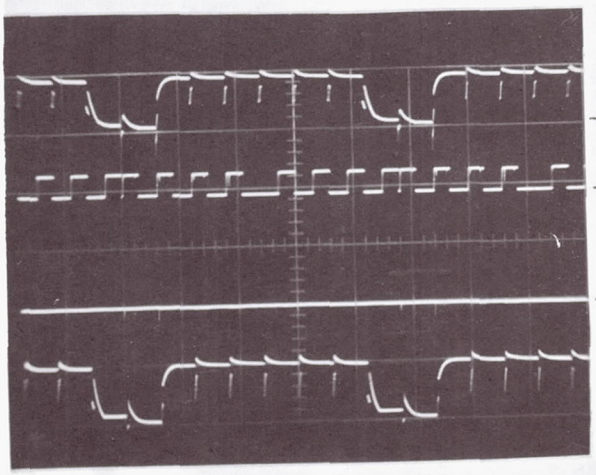
Sync Bus, (TP 10) (10V/Div.)

SUSS, (TP 14) (20V/Div.)

$\overline{SUSS} \cdot (\overline{LBC\text{-}CL})$, (TP Y) (20V/Div.)

BS No. 1, (TP X) (10V/Div.)

Startup of Subsystem No. 1 -- Initial Inverter



Sync Bus, (TP 10) (10V/Div.)

SUSS, (TP 14) (20V/Div.)

$\overline{SUSS} \cdot (\overline{LBC\text{-}CL})$, (TP Y) (20V/Div.)

BS No. 1, (TP X) (10V/Div.)

Startup of Inverter No. 1 Complete

(TP refers to test points shown in Figure 14)

Figure 32. - Startup of First Subsystem in Parallel System

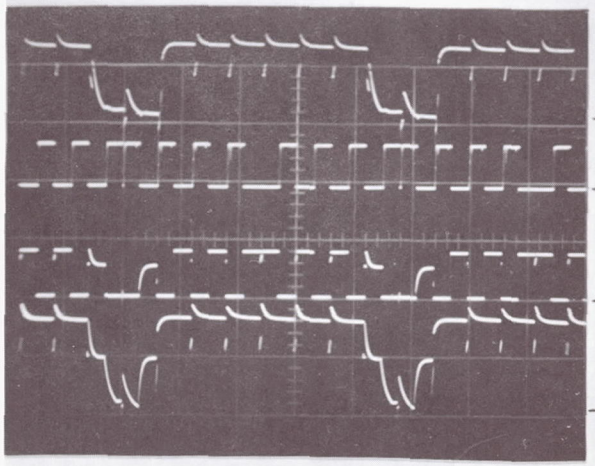
Figure 33 shows the operation of the synchronizer for an inverter being paralleled to an operating system. In this case, inverter No. 2 is being paralleled to inverter No. 1. The four traces in each picture are taken from the same test points noted in figure 39 except the last two traces are located in inverter No. 2 rather than inverter No. 1.

The upper picture of figure 33 shows the operation of the synchronizer as inverter number 2 is started. Note that signals are available at each test point. If the fourth trace of this picture is compared with the similar trace of figure 39, one sees that the blanking signal of the oncoming inverter is increased in length, i.e., the desired signal for inverter startup is present to ensure that the oncoming inverter (No. 2) is in phase with the parallel system (inverter 1). The blanking signal is developed by the combination of the sync-bus signal (trace 1) and SUSS gated through the NOR gate (trace 3). Note that the SUSS and sync signal are generated by the paralleled inverters since the logic that generates these signals within the inverter starting up (No. 2) is inhibited by control signals from the LBC and the TBC. The blanking signal of the inverter starting up is therefore forced into phase with the parallel system.

The waveforms of the synchronizer after inverter No. 2 is paralleled to the system are shown in the lower picture of figure 33. All traces of this picture are taken from the same test points as those of the upper picture. Trace 3 of the lower picture shows that the SUSS is no longer gated to the blanking signal of inverter No. 2 because the control signal, LBC-CL, has been removed. The blanking signal, trace 4, is therefore returned to its normal state and is gated to the sync bus. At this point, inverter No. 2 has as much influence over the phase of the parallel system as does inverter No. 1.

Figure 34 shows the operation of the subsystem contactors and terminal voltage as one subsystem is paralleled to another. Figure 34 shows the operation of paralleling subsystem 2 to subsystem 1. The upper traces show that all the contactors of subsystem 1 are closed and that the terminal voltage is at rated conditions. Subsystem 2 is started by closing ICC No. 2 (not shown); after 4.9 seconds inverter No. 2 builds up to normal voltage, and shortly thereafter LBC No. 2 is closed. Inverter No. 2 is now connected to its load bus and TD7 of the C/P circuits is initialized. After 1.33 seconds the TBC is closed and the two subsystems are paralleled. Each subsystem load bus is loaded at one amp unity power factor for this test.

Table XI shows the steady-state loading conditions for three loading conditions. Note that the current is shared between the inverters within the 10 percent of rated current conditions (0.21 amperes).



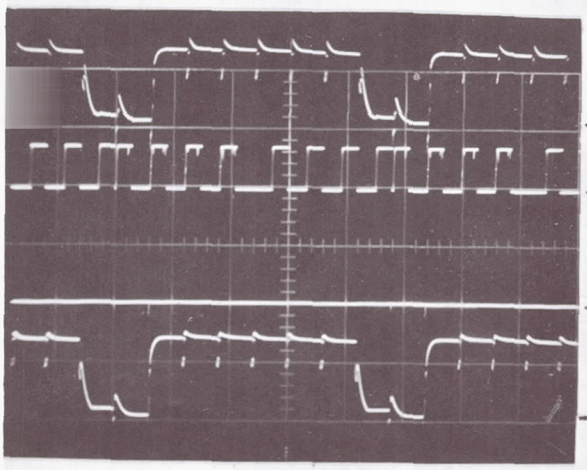
Sync Bus, (TP 10) (10V/Div.)

SUSS, (TP 14) (20V/Div.)

$\overline{\text{SUSS}}$.($\overline{\text{LBC-CL}}$), (TP Y) (20V/Div.)

BS No. 2, (TP X) (10V/Div.)

Startup of Subsystem No. 2



Sync Bus, (TP 10) (10V/Div.)

SUSS, (TP 14) (20V/Div.)

$\overline{\text{SUSS}}$. ($\overline{\text{LBC-CL}}$), (TP Y) (20V/Div.)

BS No. 2, (TP X) (10V/Div.)

Startup of Inverter No. 2 Complete

(TP refers to test points shown in Figure 14)

Figure 33. - Startup of Succeeding Subsystems

Figure 34. - Automatic Paralleling Inverter No. 2 to Inverter No. 1

Table XI. - Inverter Load Division During Automatic System Operation

Condition	A		B		C	
	Inv. #1	Inv. #2	Inv. #1	Inv. #2	Inv. #1	Inv. #2
Output Voltage (volts)						
Phase A	114.6	114.7	--	--	116	115.3
Phase B	114.6	114.3	--	--	114.8	114.3
Phase C	115.0	115.7	--	--	117.2	116.2
Output Current (amps)						
Phase A	1.92	2.0	1.55	1.53	1.95	2.0
Phase B	1.85	2.0	1.54	1.45	1.95	1.93
Phase C	1.84	2.03	1.56	1.48	1.98	1.92
Output Power (watts)						
Phase A	220	228	135	133	168	166
Phase B	214	232	137	133	172	174
Phase C	210	232	141	127	174	163
Approximate Power Factor	1	1	0.77	0.76	0.75	0.71
Input Voltage (volts)	27.5	27.5	--	--	27.6	27.6
Input Current (amps)	37.9	35.7	--	--	26.7	27.7
C/P Current (amps)	0.27	0.25	--	--	0.27	0.25

Load-division protection test: These tests demonstrate that the load-division protection circuit trips the TBC if the current unbalance between inverters exceeds 0.4 amperes (20 percent of rated current). The first test was to determine the trip point of the load-division protection circuit. Table X lists the trip point. The trip point was established by forcing each subsystem to operate isolated but maintaining operation of the load-division control and protection circuits. The load on one system was varied such that there was a difference in inverter output current. The test was run at both unity and 0.75 lagging power factor. The protection circuit operated independent of load power factor.

A load-division fault test was also run with the inverters paralleled. The fault was applied by shorting the terminals of the load-division current transformers. The load-division circuits were thus prevented from forcing the inverters to share load; i.e., the inverters divided load according to their natural voltage-current characteristic. Figure 35 shows the result of this fault. Figure 35 shows the TBC in inverter subsystem 2 tripping. Since only two subsystems are present, one trip effectively makes the load-division control and the load-division protection circuits of both subsystems inoperative. To show that

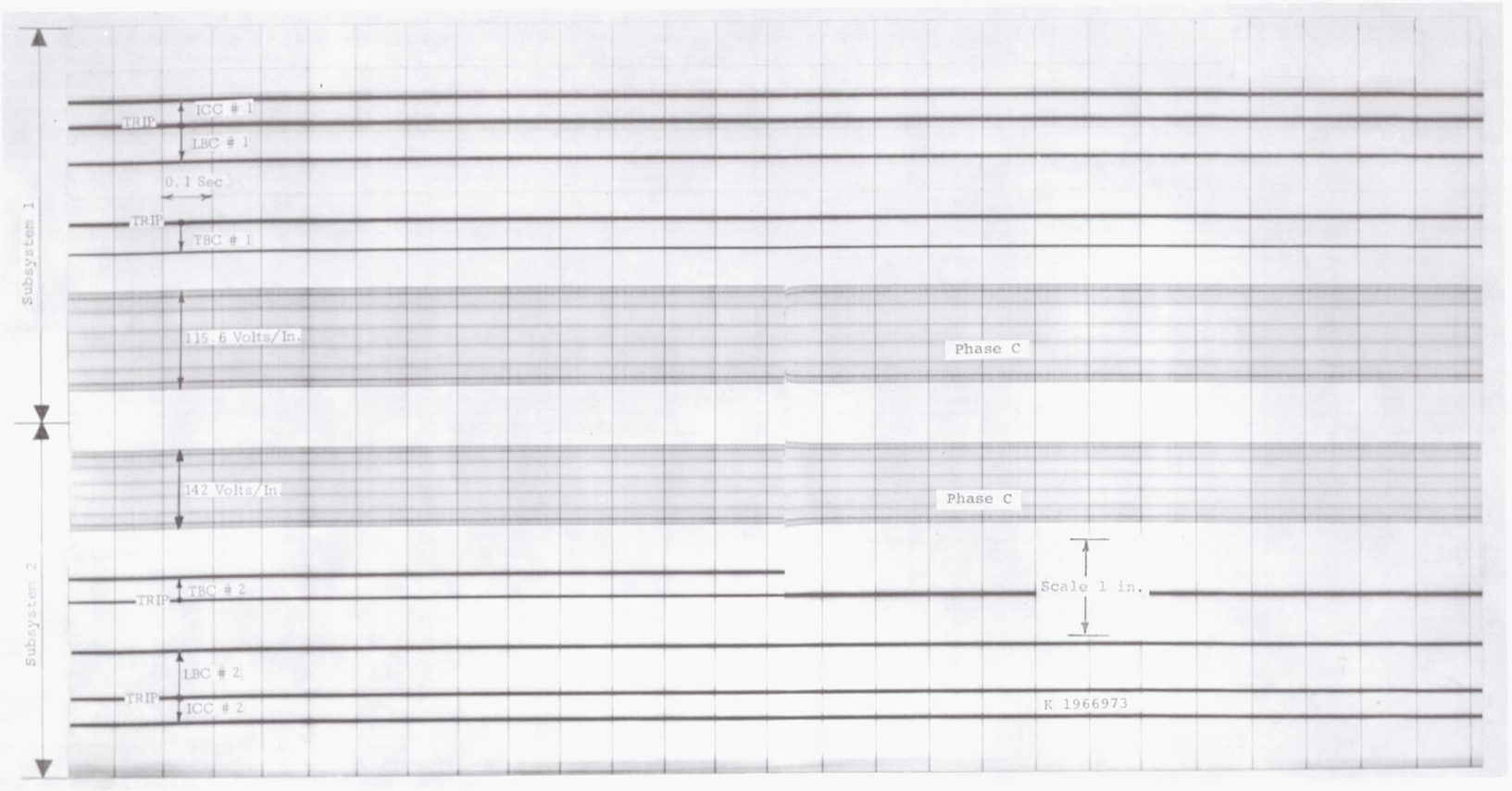


Figure 35. - Parallel Inverter System, Load-Division Fault, Shorted Load-Division Current Transformer

both LDP circuits operate, the LDP circuit in subsystem 2 was disabled so that the LDP in subsystem 1 could operate.

The load-division protection circuit sensed the fault condition and tripped the TBC as required. Selective tripping of the TBC in a two-inverter parallel system is not necessarily required (and is not provided in these circuits) since opening either TBC effectively isolates the subsystems and prevents the load-division protection and load-division control circuits from operating. The section on "Inverter Control and Protection Circuit Design" describes how selective tripping can be accomplished when three or more inverters are paralleled.

Load-bus overcurrent protection (Zone 2): This test demonstrates that the control and protection sensing and logic circuits can locate and isolate an overcurrent fault. Table X shows the measured trip points of the inverter and load-bus over-current sensing circuits. A load-bus overcurrent fault causes both overcurrent sensing circuits in a faulted subsystem to have an output. Thus, time delays TD3, TD4, and TD5 are initiated. Figure 36 shows that the protection circuits provided the proper signals to locate and isolate a faulted load bus. The lengths of TD3 and TD5 are shown by the trip indications of the LBC and the TBC, respectively. Note that TD4 on the unfaulted system did not cause its TBC to trip.

Figure 36 shows the result of a fault on load bus No. 1. The traces of the upper half of the oscillograms show the operation of subsystem 2 while those of the lower half show the operation of subsystem 1. The application of the fault is noted by the sudden rise in phase current. The parallel system supplies current to the fault for 0.235 second at which time TBC No. 1 trips. Since this action isolates the fault from subsystem 2, the current in subsystem 2 returns to normal limits. However, the action of tripping TBC No. 1 does not remove the fault from inverter No. 2 as is indicated by the continued overcurrent. Since the fault is not removed, TD5 in the C/P circuits of subsystem 1 continues to time out and after 0.517 second, LBC No. 1 trips removing inverter No. 1 from load bus No. 1. The faulted load bus is now isolated from the parallel system and its associated inverter.

This shows that the C/P circuits provide proper operation to isolate a faulted load bus in a parallel system.

Tie-bus overcurrent protection (Zone 3): This test demonstrates that a fault on the tie bus isolates all subsystems from the tie bus but does not shut down a subsystem. Since all subsystem load busses are unfaulted, only the inverter overcurrent

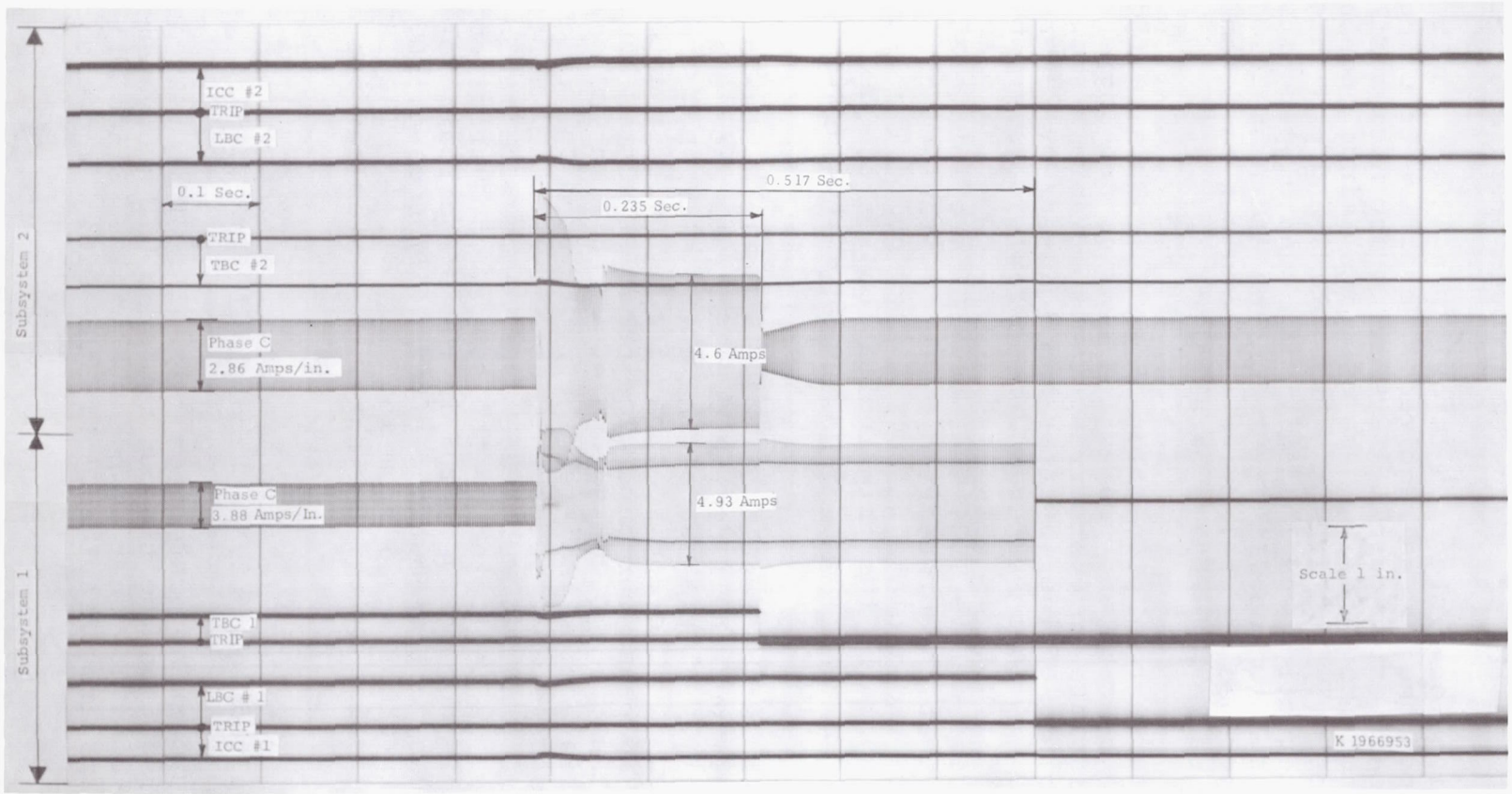


Figure 36. - Parallel Inverter System, No. 1 Load-Bus Fault, Phase C to Ground

protection circuit has an output. TD3 and TD4 in each C/P circuit are, therefore, the only time delays initiated. Figure 37 shows the results of a three-phase fault on the tie bus. The length of TD4 is noted by the trip indication of the TBC. Time delay TD3 did not time out because the opening of the TBC removed the inverter overcurrent condition.

This oscillogram shows that the control and protection circuits provided the proper system operation.

Differential current protection (Zone 1): Zone 1 includes the distribution system from the neutral of the inverter to the load-bus contactor. The control and protection must sense when the fault current in Zone 1 is greater than 1.3 amperes and shut down the associated inverter. Figure 38 is an oscillogram of system operation during this fault. Table X shows the trip point for each differential current protection circuit. Figure 38 shows the results of a three-phase fault applied to Zone 1 of subsystem 2. The fault application is indicated by the sudden rise in phase current. After 0.009 second, subsystem 2 is de-energized by tripping ICC No. 2 and LBC No. 2. The parallel system then assumes the load of load-bus No. 2 as indicated by the increase in current of phase C of subsystem 1.

The control and protection circuits provided the proper system operation under all combinations of faults within the differential current protetion loop (Zone 1).

Frequency reference failure: This protection is primarily for the reference oscillator because all inverters are operated from a single reference source. Therefore, a single failure will affect the operation of the whole system. The approach to this circuit was to sense a fault and transfer to a new reference source as quickly as possible without affecting parallel system operation. The tuning fork is assumed to fail in either of two modes: direct voltage or a frequency below 1800 Hz. The method of fault detection is described in the "Inverter Control and Protection Circuit Design" section. Simulated faults were applied to the tuning fork output. The reaction time of the protection and transfer circuit is shown in figure 39. Note that the failure time is less that 1/3200 seconds. A fault of this nature causes a voltage phase shift of from 0 to 45 electrical degrees depending on the slip position of the two tuning forks at the time of transfer.

The circuit provides the necessary protection for failures of the reference frequency oscillators. However, the C/P circuits do not provide for selective protection for failures occuring within the inverter countdown circuits or the power circuits.

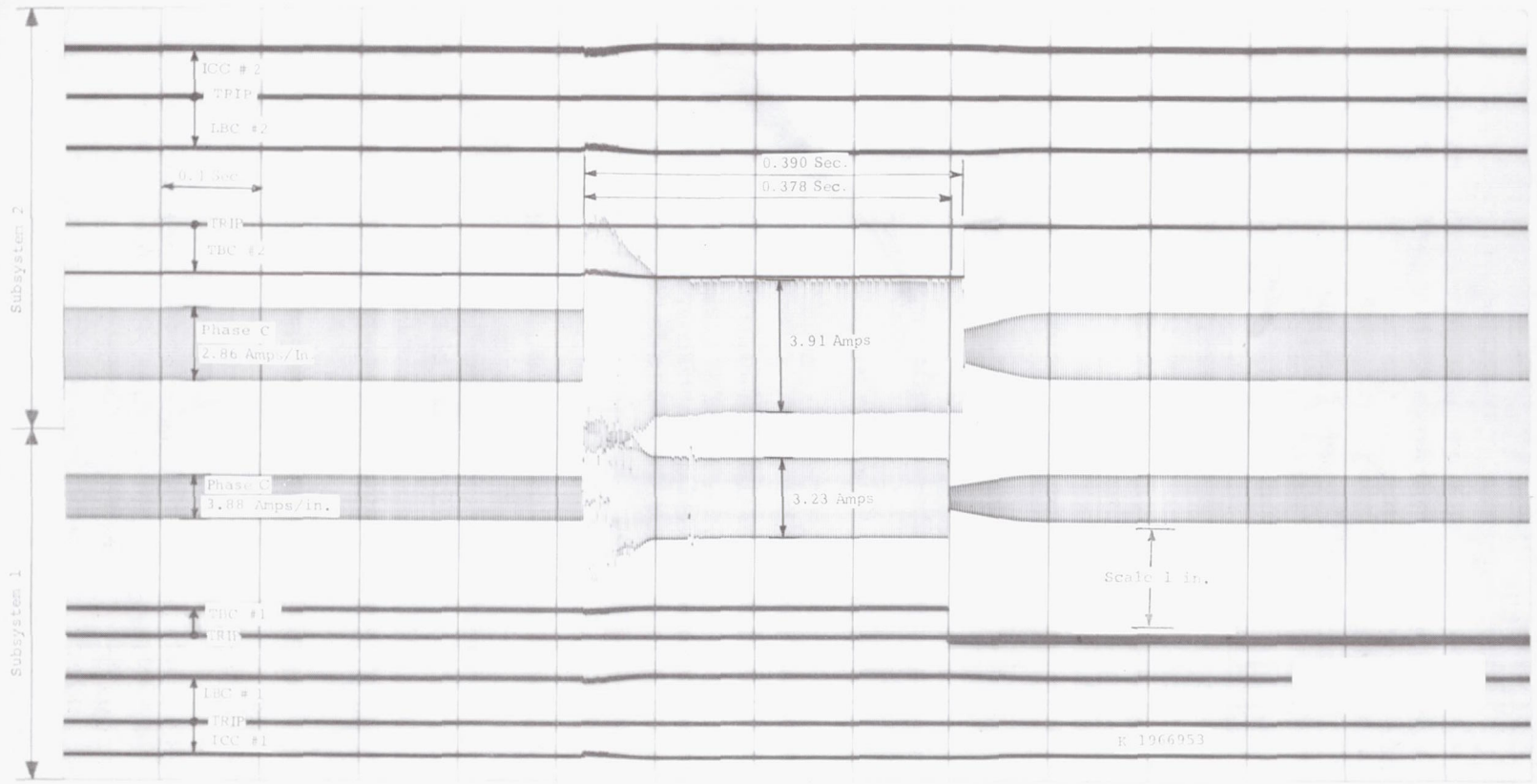


Figure 37. - Parallel Inverter System, Tie-Bus Fault, Three-Phase

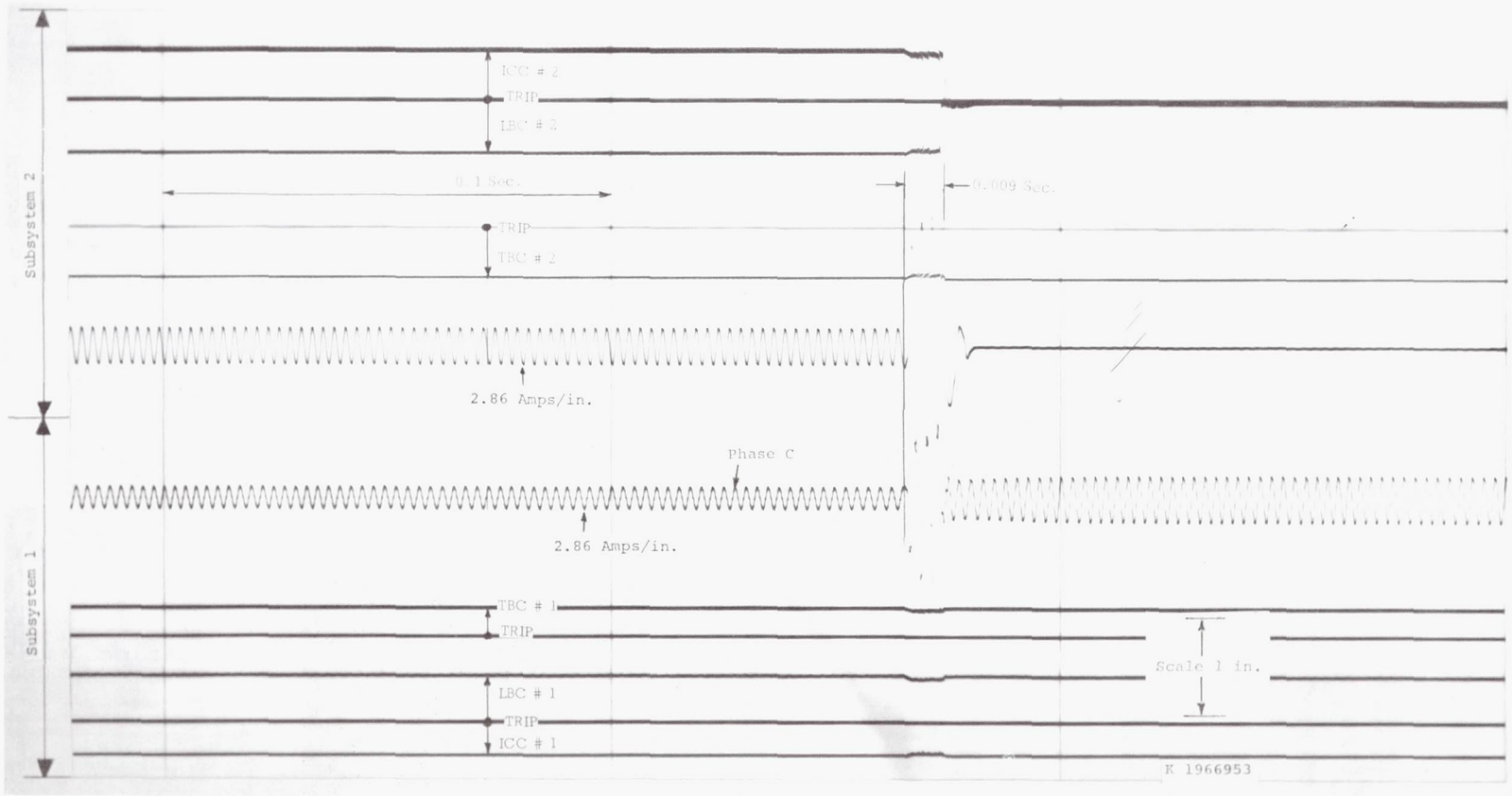
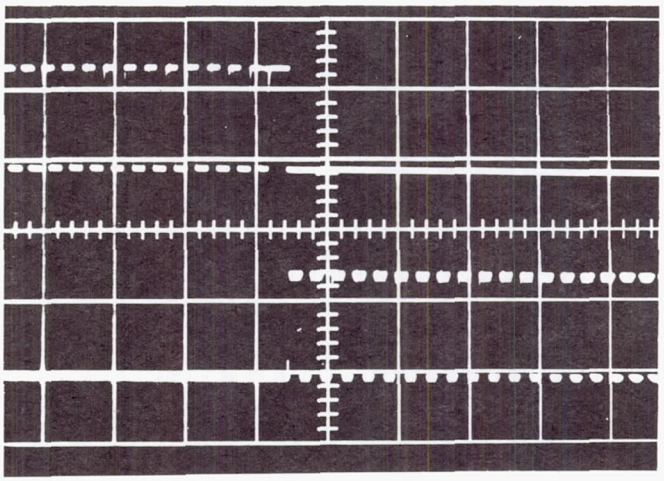


Figure 38. - Parallel Inverter System, Zone 1 Fault on Subsystem No. 2, Three Phase

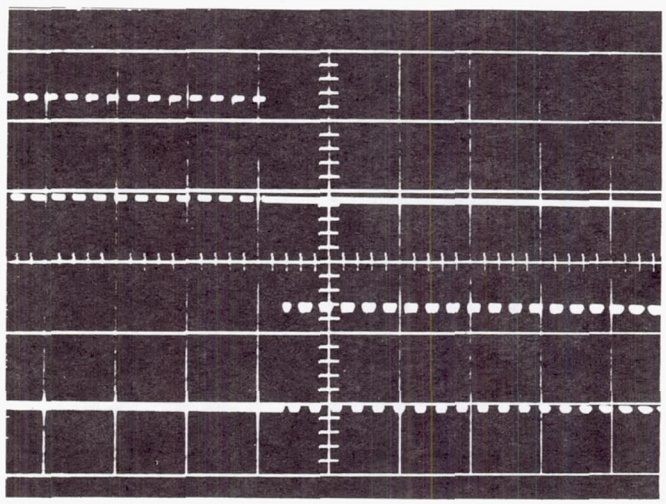


Upper Trace:
TUNING FORK NO. 1

Lower Trace:
TUNING FORK NO. 2

Timing:
Waveforms are:
3200-Hz square waves

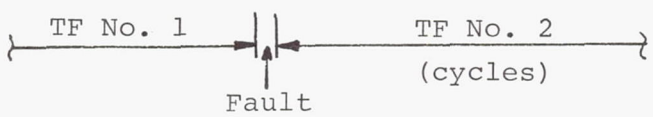
TUNING FORK FAULT-ZERO OUTPUT VOLTS



Upper Trace:
TUNING FORK NO. 1

Lower Trace:
TUNING FORK NO. 2

Timing:
Waveforms are:
3200-Hz square waves



TUNING FORK FAULT--PEAK OUTPUT VOLTS

Figure 39. - Tuning Fork Reference Fault Protection

These types of failure protection were beyond the scope of this program. Failures of this type would result in either frequency variations or voltage changes. The load-division protection, off-frequency, or abnormal-voltage protection circuits would trip the subsystem. Upon manual reset, the unfailed inverters would normally start up and automatically parallel while the faulted inverter would not complete startup because of a power quality fault.

Results and Analysis of Parallel Converter System Tests

Manual system operation. - The tests during manual system operation showed that the converter can be operated manually, exclusive of all automatic control and protection. Further, these tests demonstrated that the basic performance of a parallel converter system is unaffected by the addition of the automatic control and protection circuit.

The manual mode of operation was selected by placing the manual override switch in the MANual position. A startup operation was then attempted by placing the Converter Control Switch in the CLOSE position. The CCC did not close, the converter did not start, and no dc power was provided to energize the automatic protection and paralleling circuits.

The CCC Manual Control Switch was placed in the CLOSE position. The CCC closed and the converter was energized. However, neither the LBC nor the TBC operated to connect the converter to the subsystem load bus or to the system tie bus.

The subsystem LBC was then closed (connecting the converter to the subsystem load bus) by placing the LBC manual control switch in the CLOSE position. The Converter Control Switch was placed in the TRIP position, attempting to trip the CCC and the LBC. Neither action occurred.

The subsystem was then connected to the system tie bus by placing the TBC manual control switch in the CLOSE position, closing the TBC. The Converter Control Switch was placed in the TRIP position attempting to trip the CCC, LBC, and TBC. None of the contactors operated.

During system operation, the converter output voltage was adjusted to 120 volts, an undervoltage condition, and then increased to 170 volts, an overvoltage condition. The automatic abnormal voltage protection did not operate, and the abnormal voltage condition remained until it was again adjusted to 153 volts.

Direct faults to ground were applied within Zone 1 at the converter output, within Zone 2 at the subsystem load bus, and within Zone 3 at the system tie bus. The load-bus or tie-bus fault protection circuits did not operate.

With one subsystem operating, the second subsystem was started and connected to the subsystem load bus and the system tie bus manually paralleling the two subsystems. The second subsystem was disconnected from the system tie bus by placing the TBC manual control switch in the TRIP position and its voltage adjusted to 120 volts. A 2.5-ampere load was applied to each subsystem's load bus. The No. 2 subsystem was then connected to the system tie bus by placing the TBC manual control switch in the CLOSE position. No operation of either the automatic paralleling circuit to prevent connection of the No. 2 subsystem to the tie bus or of the automatic load division protection circuit to trip the system tie-bus contactor occurred. Subsystem No. 1 supplied the total load of 5.0 amperes.

The manual load-division control switch (S7 in figure 16) was then closed. The converters immediately shared load current within the allowable 10 percent variation.

The subsystems were disconnected from the system tie bus by placing their respective TBC manual control switches in the TRIP position. Then each converter was isolated from its load bus by placing the subsystems LBC Manual Control Switch in the TRIP position. Each subsystems converter was then de-energized by placing the subsystems CCC manual control switches in the TRIP position.

The manual system operation test demonstrated that the automatic protection and paralleling circuits are not operative during manual system operation and that system operation is not affected by the control and protection circuits.

Automatic single subsystem tests. - The purpose of this series of tests was to show the automatic operation of a single subsystem under normal and abnormal operating conditions. The "Converter Control and Protection" section of this report describes how the system should operate.

Automatic system startup and effect of manual control: This test demonstrated that the manual switches exercise no control over the system when the manual override switch is in the AUTOmatic position.

First, all contactors were placed in the TRIP position and both manual override switches were placed in the AUTOmatic position. An attempt was made to start each subsystem and to close its contactors by operating the CCC, LBC, and TBC manual control switches. The contactors would not operate.

Each converter was started by placing its Converter Control Switch (CCS) in the CLOSE position. The converter reached a power-ready condition, and the load-bus and tie-bus contactors closed automatically. Each manual control switch was placed in the TRIP position, but the contactors still would not operate. The converter was shut down by placing the CCS in the TRIP position. All contactors were immediately tripped.

These tests showed that all manual controls are inoperative when the manual override switch is in the AUTOmatic position, whether the converters are operating or not.

Automatic system startup, no-power-ready condition: This test demonstrated that a converter will not automatically complete the startup sequence should one of the power-ready conditions not be met. The power-ready condition is that the terminal voltage of the converter must be within the ranges listed in table XII.

Table XII. - Measured Trip Points of Converter Automatic Protection Circuits

CIRCUIT	RANGE		MEASURED	
	Lower Limit	Upper Limit	C/P #1	C/P #2
Overvoltage (OV), volts	157	163	163	162
Undervoltage (UV), volts	138	142	144	142
Differential Current (DP), amps	0.20	0.75	Fig. 42	Fig. 42
Tie-Bus Overcurrent (TBOC), amps	5.4	5.9	5.85	5.9
Converter Overcurrent (COCP), amps	5.4	5.9	5.8	5.8
Load Division Protection (LDP), amps	0.49	1.0	Fig. 41	Fig. 41
Time Delays (Seconds)				
TD1	6.3	7.7	8.6	8.1
TD2	0.16	0.24	0.17	0.19
TD3	0.99	1.21	1.15	1.10
TD4	0.20	0.30	0.23	0.26
TD5	0.20	0.30	0.22	0.20
TD4 + TD5	0.40	0.60	0.45	0.46
TD6	0.10	0.15	0.11	0.11
TD7	0.16	0.24	0.41	0.30
TD8	0.60	0.90	0.81	0.81

Under an automatic startup condition, the converter is started by closing the converter control contactor (CCC). The converter output remains zero for about five seconds. At the end of this time delay, the output voltage will rise to a given value. If the power quality is within the limits specified in table XII, the LBC will close, stopping the no-power-ready time delay.

Ultimately, if conditions are proper, the TBC will close. If, however, the power quality is outside the limits of table XII, the LBC should not close, the CCC should trip, and the TBC should close after the no-power-ready time delay times out.

Figure 40 shows the operation of subsystem 1 under a no-power-ready condition. The upper traces of the oscillogram show the state of the contactors and the terminal voltage and current of subsystem 1. The load-bus and tie-bus contactors are closed when a trace appears below the trip line of the oscillogram. The end of the arrow indicates where the trace should appear. The CCC is closed when a trace appears above the trip line as indicated by the arrow.

The terminal voltage and current traces on the oscillogram have a common zero. Positive current is indicated by a trace above the zero line; whereas, positive voltage is indicated by a trace below the zero line. For this fault, then, the CCC is closed (not shown) and after 5.13 seconds, the converter builds up. After the initial startup transient the terminal voltage is 131 volts, which is below the required 153 volts and within the limits of the UV sensor. The LBC does not close and after a total of 8.6 seconds, the no-power-ready time delay trips the CCC and closes the TBC connecting load bus No. 1 to the system tie bus.

Comparison of the measured length of the no-power-ready time delays with the limits established in table XII shows that the time delay is longer than desired. The cause of this was that the R42, figure 16, in the shunt regulator was too large causing the regulated voltage to droop below 15 volts. The lower reference voltage increases the time for the capacitor in the RC time delays to reach the reference Zener diode voltage. Through an oversight, new oscillograms were not taken. The subsystem operation due to the lengthened time delay is not impaired, however, because the effect of the longer time delay only allows more time for the converter to provide power of the proper quality.

Power quality fault during isolated operation: This test showed that abnormal voltage circuits provide protection for converter faults occurring during single subsystem operation. The OV and UV sensing circuits provide signals to a nominal 1.1-second time delay (TD3) which trips the CCC and LBC contactors and provides a close signal to the TBC. Table XII lists the calibration of the OV and UV sensing circuits.

The oscillogram of figure 41 shows the result of an overvoltage fault on a single subsystem (No. 2). The subsystem is operating normally and an overvoltage fault is applied as evidenced by the rise in terminal voltage. (These charts are read

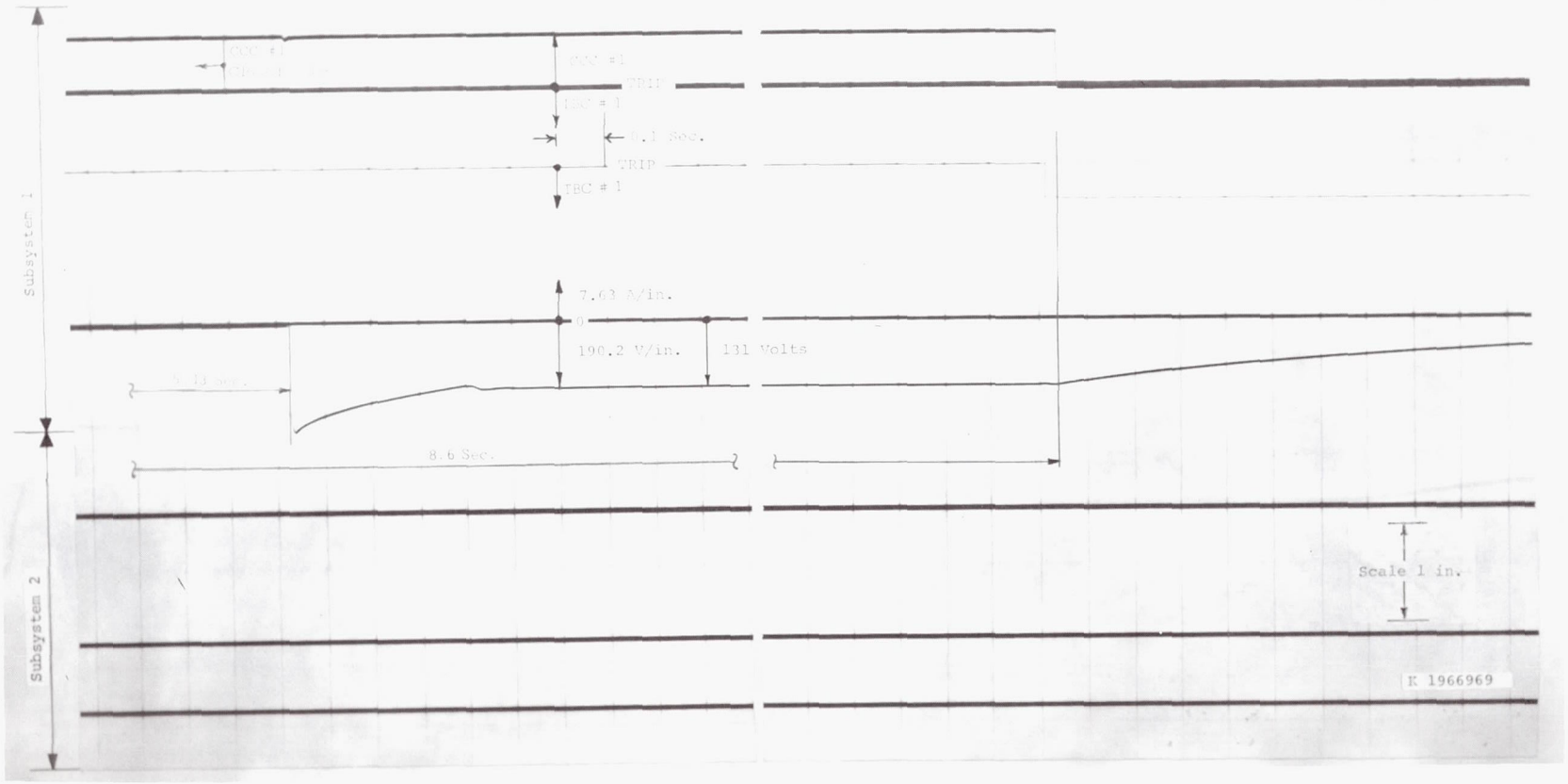


Figure 40. - Converter System No. 1 - Isolated, Start-up with Undervoltage Fault

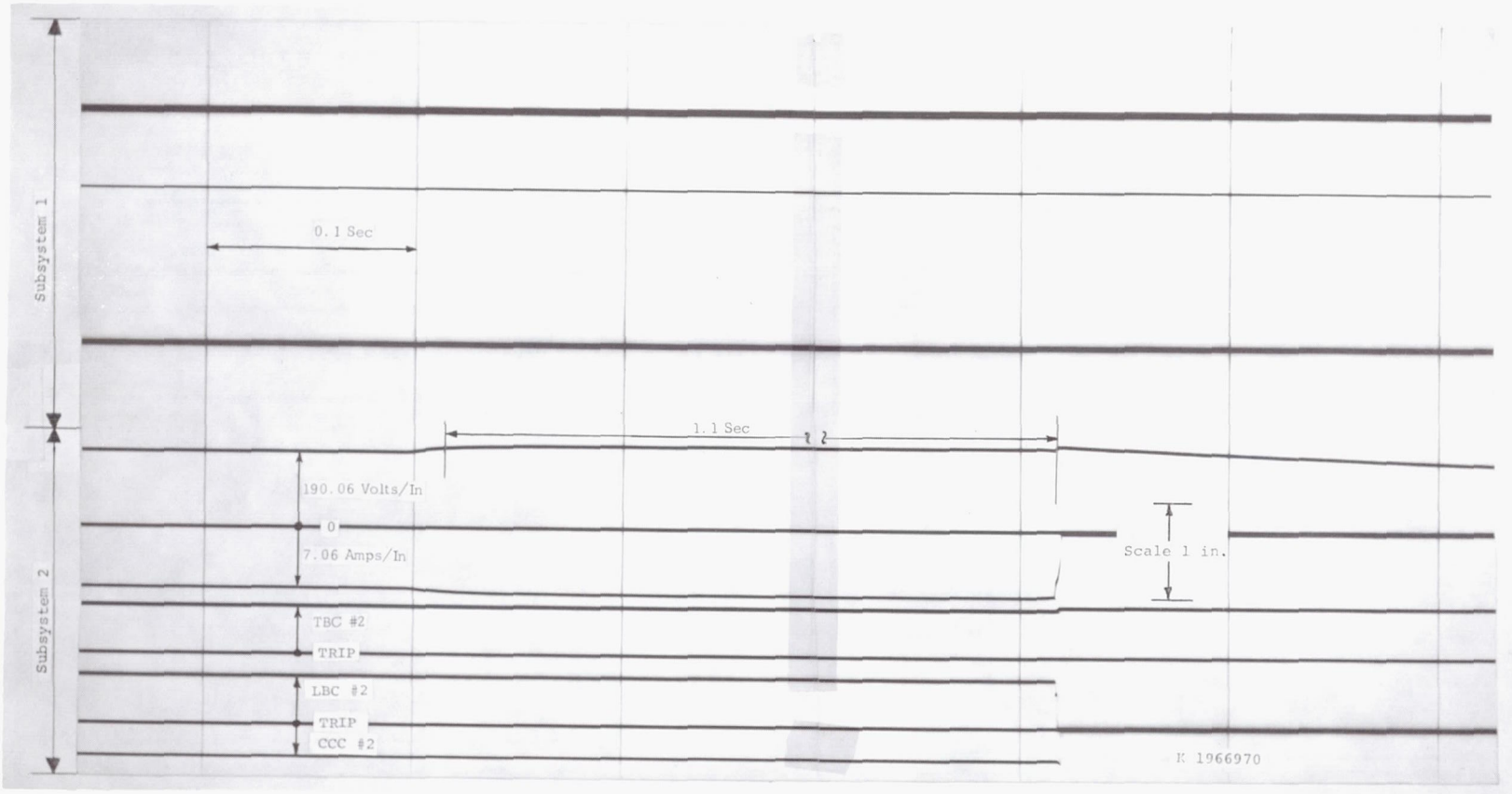


Figure 41. - Converter System No. 2 - Isolated, Overvoltage Fault

like figure 40.) The fault continues for 1.15 seconds at which time delay TD3 trips both the LBC and CCC shutting down the inverter. This is indicated by the output current being reduced to zero and the terminal voltage slowly decaying to zero. The slow decay in terminal voltage is due to the charge on the output filter capacitor.

The subsystem C/P circuit provides proper operation for either OV or UV faults and the action was accomplished within the tolerance of time delay TD3.

Differential current protection (Zone 1): This test demonstrated the protection provided for a Zone 1 (see figure 1) fault. The differential current protection circuit operates immediately to trip the CCC and the LBC. Table XII and figure 42 show the variation in trip point as a function of load current. Note that the limits are exceeded for load currents below 1.5 amperes.

There are two reasons for this variation. One is the nonlinearity in the output voltage of the transductor circuit for load currents near zero. The other is the nonlinearity in output voltage of the differential amplifier. The output voltage characteristic of the transductor circuit is shown in figure 43. The slope of the curve is not steep and not linear near zero load current. For load currents near zero, the difference in output voltages of the transductor circuits is small. This results in small difference in the voltage applied to the bases of the differential amplifier transistors and a small output voltage from the differential amplifier. Therefore, a larger differential current is required to operate the protection circuit. When the transductor circuits are operating at a higher level of current, the output characteristics of the transductor circuits are operating on the steeper portion of the transductor output curve. A smaller difference in currents then results in a larger difference in input voltage to the bases of the transistors of the differential amplifier. This increases the output voltage of the differential amplifier and results in a lower operating point for the DP circuit. This condition results in a non-linear output of the differential amplifier with load causing the differential protection circuits trip point to vary with load.

The differential amplifier also adds to the nonlinearity of the differential protection circuit at the lower values of load current. This is a result of the variation in gain characteristics of two transistors in the differential amplifier. The gain of the transistors increases with collector current. At lower base voltages the transistor gain is lower, and a lower output voltage is provided by the differential amplifier. This also requires a larger difference current to operate the differential

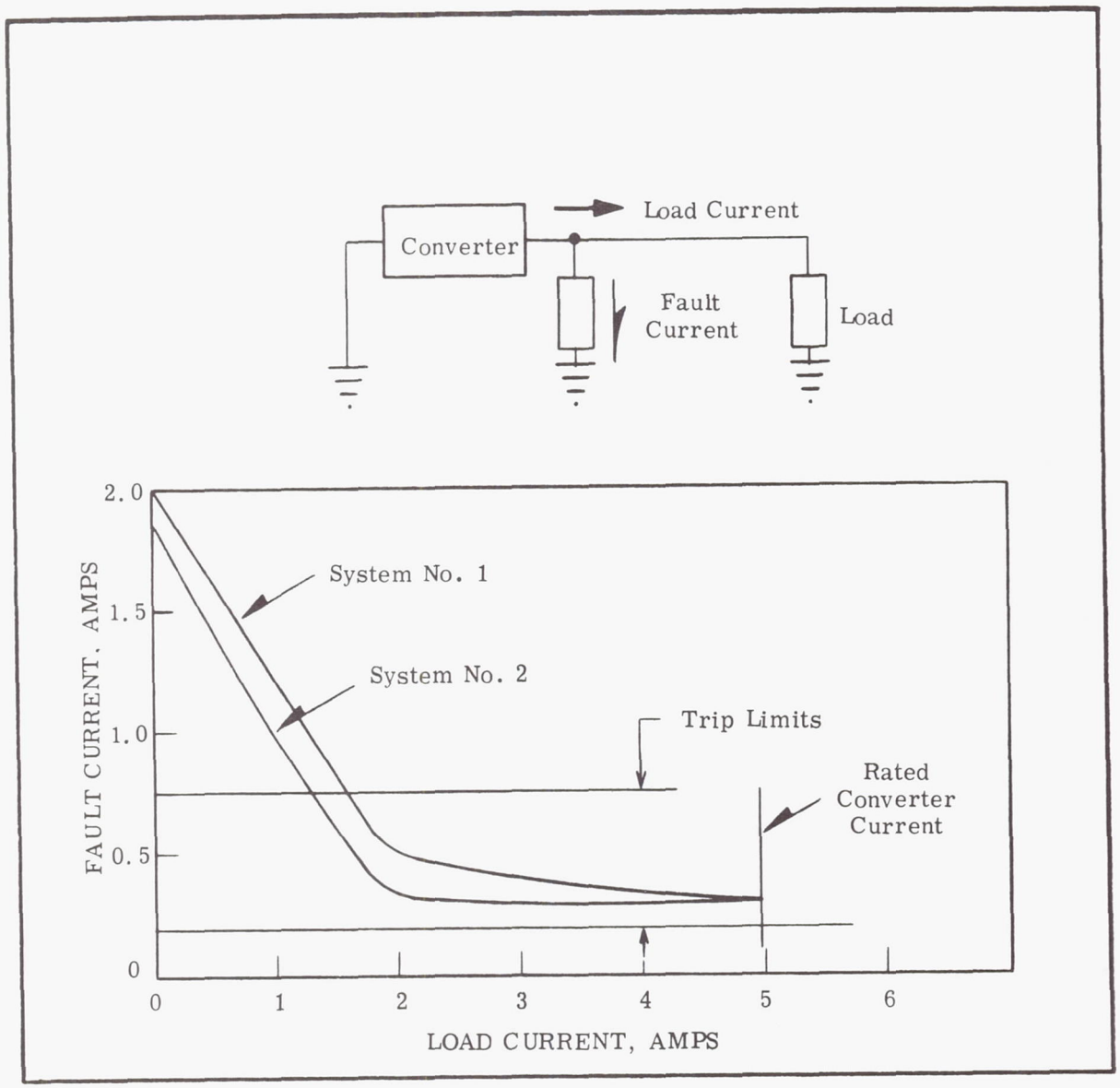


Figure 42. - Characteristics of Differential Protection Circuits

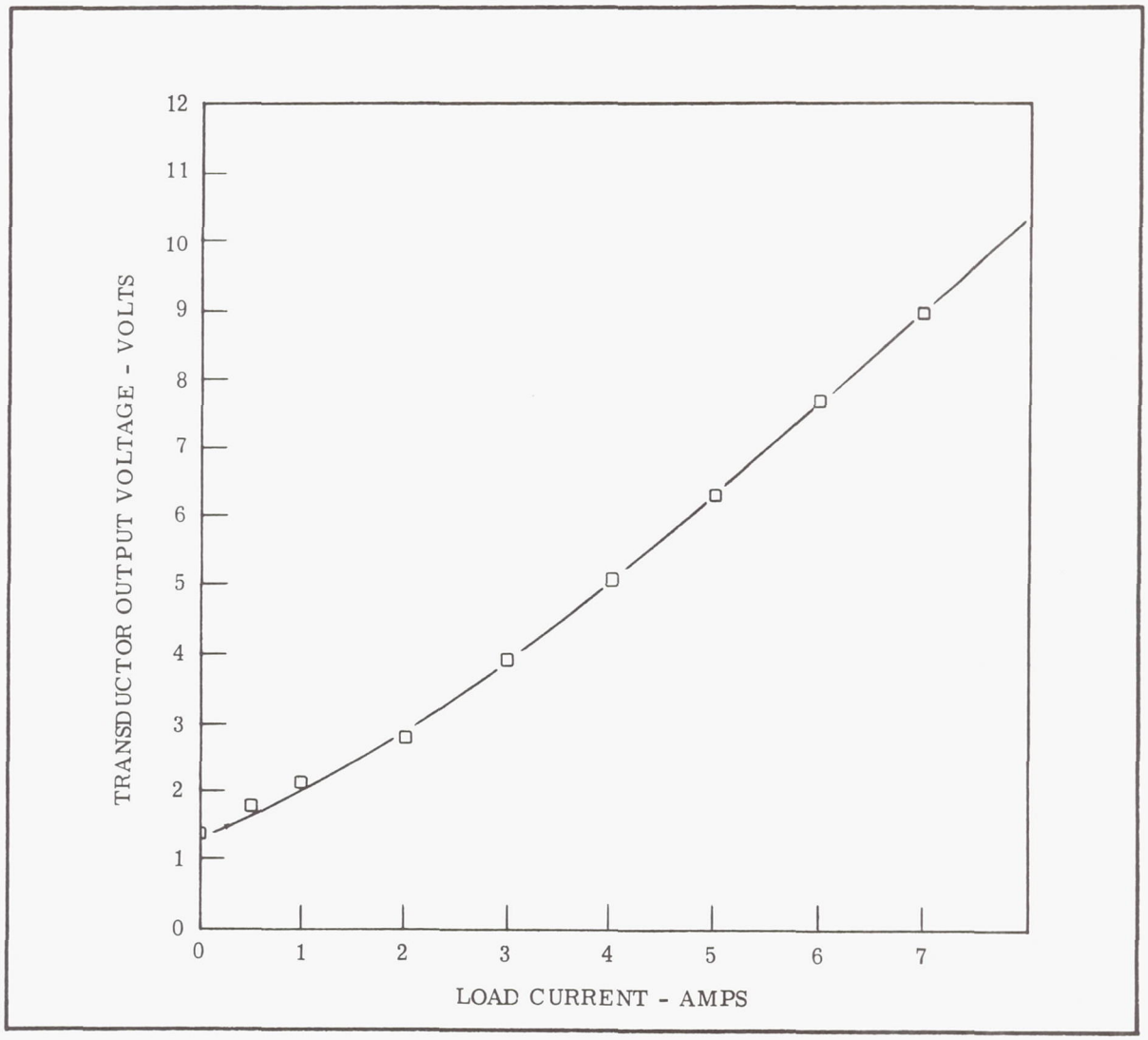


Figure 43. - Output Characteristics of the Differential Protection Transductor Circuit

protection circuit. At higher operating values of load current, a larger voltage is applied to the base of the transistors, and they operate in an area of higher gain. This results in a large output voltage from the differential amplifier for the same differential current.

To minimize the nonlinearity of the differential protection circuit, the transductor circuit must be redesigned to provide a more linear output at the lower current levels. The differential amplifier should also be modified to use transistors matched with respect to gain and with less variation in gain with base drive.

The circuit was not modified to eliminate the variation of the DP sensing circuit trip point because the intent of the circuit was demonstrated. Further, this type of operation might be advantageous for some applications since the decrease in sensitivity occurs only at light load. Figure 42 shows that the maximum differential current (fault current) occurs at zero load current and is less than 50 percent of rated current. This means that the converter with a DP fault and no load current is at only 50 percent load. Another point for not modifying the circuit at this time is the fact that the specification for the DP sensing circuit for the inverter system trips at a fault current equivalent to 50 percent of rated current. Therefore, even though the converter DP sensing circuit is outside the limits set for it, the circuit does ensure that an overcurrent beyond the rating of the converter is not sustained.

The response of the DP circuit is shown in figure 44. The traces on figure 44 are read the same as those of figure 40. Note that all three contactors are closed at the time the DP fault is initiated. The fault is initiated by the sudden rise in current. The average fault current is 13.5 amperes and the fault continues for 0.03 seconds at which time both the LBC and ICC are tripped.

These oscillograms show that the converter C/P circuits provide proper contactor control to isolate a faulted feeder (Zone 1).

Single subsystem, load-bus fault (Zone 2 overcurrent): This test deomonstrated that the C/P circuits provide protection for either a single subsystem paralleled to the tie bus or for an isolated (TBC tripped) subsystem. Figure 45 shows the result of a fault on load bus No. 1. Note that all three contactors are closed. The application of the fault is indicated by the sudden rise in current. After the initial transient the fault current is 9 amperes. After 0.228 seconds, the TBC is tripped by time delay TC4. At this time TD4 also initiates TD5. After an additional 0.22 seconds, the LBC and CCC are tripped, isolating the faulted load bus from both the converter and the system tie bus. Of course, if the TBC were already tripped the same sequence of events would occur and the LBC and CCC would be tripped, in this case, after a total of 0.448 seconds. Table XII lists the length of these time delays and the calibration of the converter overcurrent sensor.

Note that the tie-bus overcurrent sensing circuit did not initiate TD6. This would manifest itself in earlier tripping of the TBC; the tie-bus overcurrent sensing circuit is properly connected.

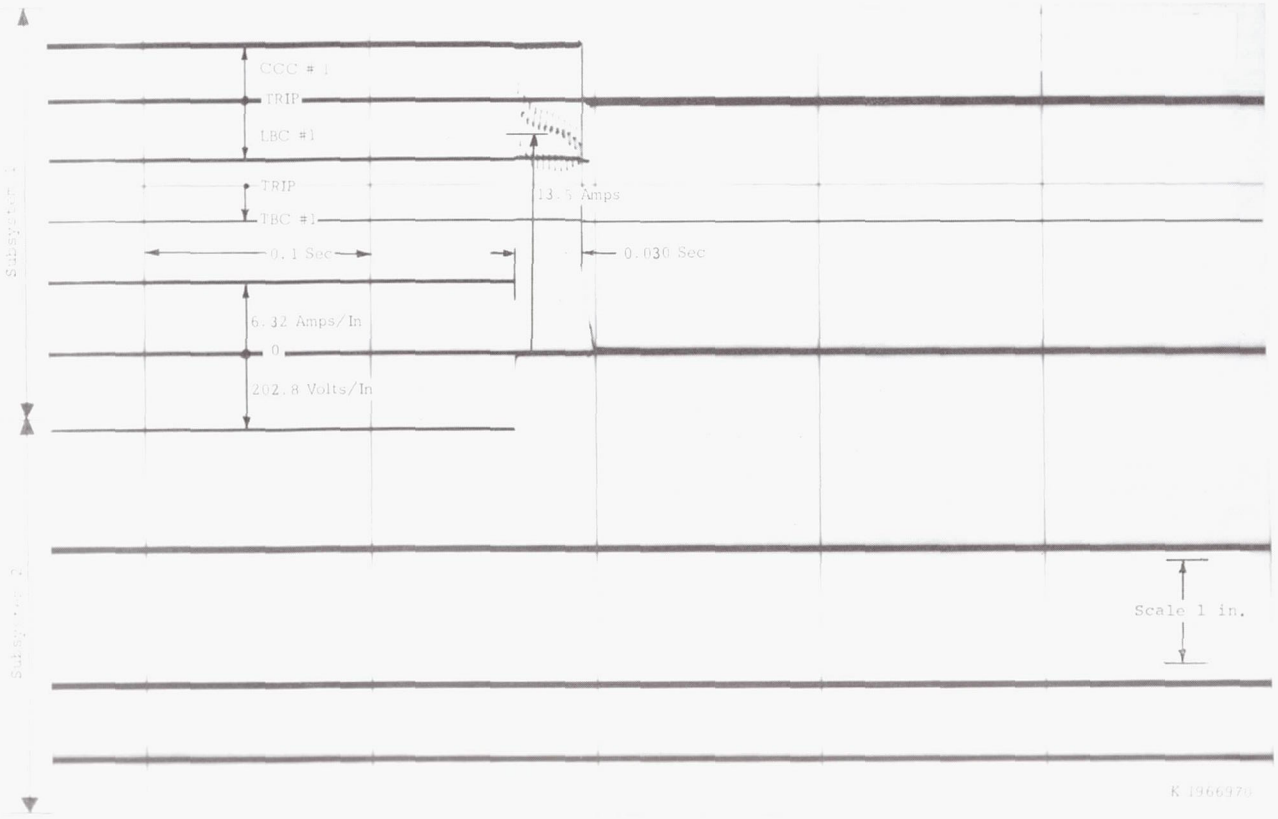


Figure 44. - Converter No. 1 - Isolated, Zone 1 Fault

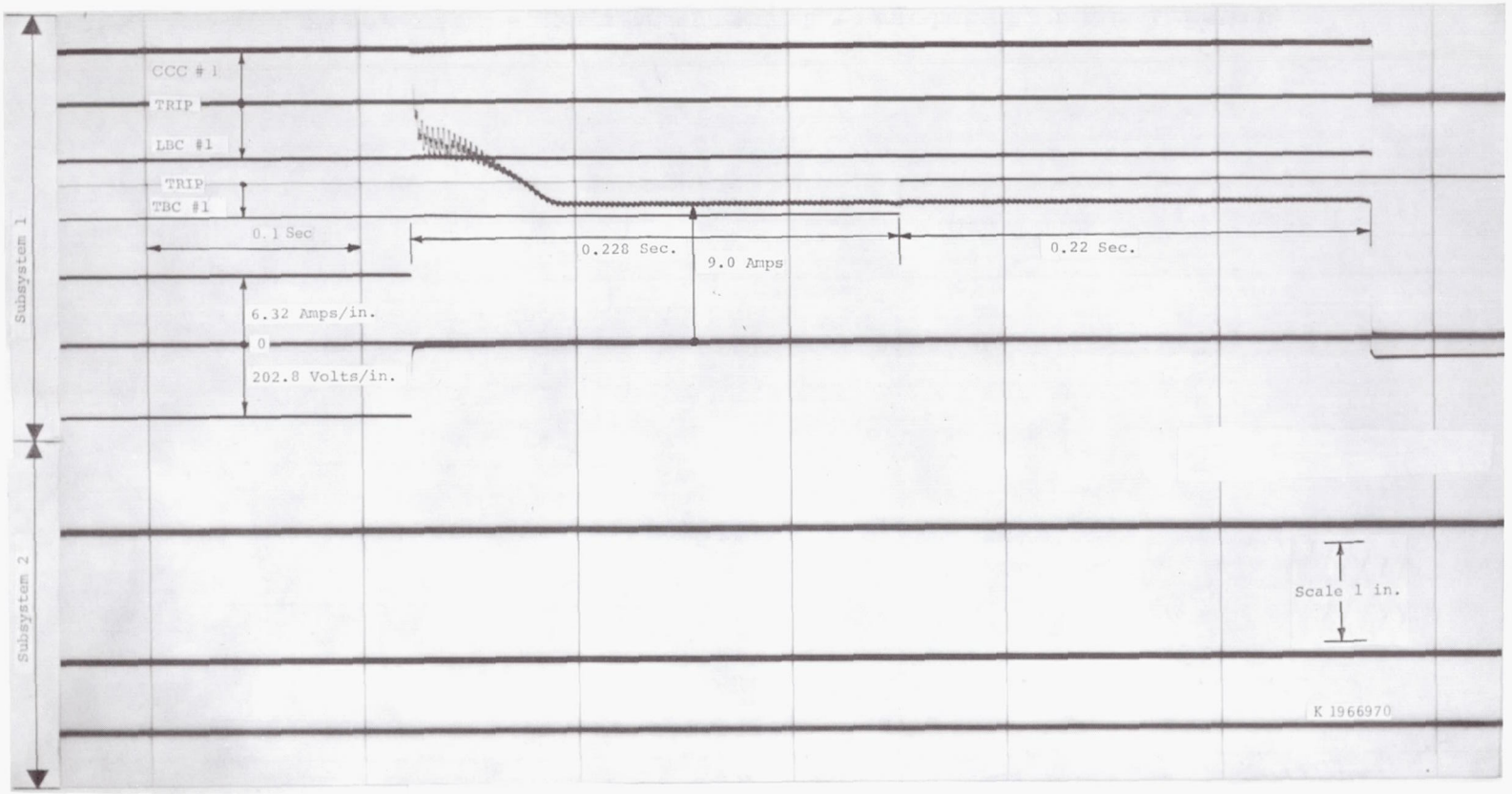


Figure 45. - Converter No. 1 - Isolated, Load-Bus Fault

The oscillogram shows that the protection circuits provide the proper operation to isolate a faulted load bus from the tie bus and the associated converter when the subsystem is operating either as a single or as an isolated subsystem.

Tie-bus fault on a single subsystem (Zone 3 overcurrent): This test demonstrated that the protection circuits can distinquish between a load-bus and a tie-bus fault when only one subsystem is connected to the tie bus. Figure 46 shows the operation of subsystem 1. The fault current for subsystem 1 is 9.1 amperes. After 0.226 seconds TD4 trips the TBC. This action removes the fault as is evidenced by the recovery in terminal voltage and the reduction in converter current to the value just prior to the application of the fault. Since the fault is removed, time delay TD5 is not initiated, and the subsystem then is operating in an isolated mode. Again, as for the load-bus fault, TD6 was not initiated and hence did not trip the TBC.

The oscillogram shows that the protection circuits provide proper operation to isolate the subsystem from the tie bus but not from its load bus under a tie-bus fault condition.

Automatic, parallel system operation. - This series of tests showed the automatic operation of a parallel converter system under normal and abnormal operating conditions. The "Converter Control and Protection" section of this report describes how the system should operate.

Automatic paralleling: The sections "Converter Control and Protection" and "Converter Control and Protection Circuit Design" describe the conditions that must be met before a subsystem can parallel to an activated tie bus. The current sharing (load division) after paralleling is indicated on each oscillogram. Load division under various steady-state loads is shown in table XIII.

Figure 47 shows the system reaction to paralleling subsystem 1 to subsystem 2. The lower traces show that all contactors of subsystem 2 are closed and that converter 2 is at nominal voltage and is supplying current to its load bus. The upper traces show the state of subsystem 1. After the CCC has been closed for 5.52 seconds, converter No. 1 builds up. After the initial build-up transient, the voltage stabilizes to nominal conditions and TD2 is initiated. This operation takes 0.5 seconds at which time the LBC is closed and the inverter begins to supply current to load-bus No. 1. TD7 is then initiated and after 0.41 seconds the TBC is closed. The converters are now paralleled and begin to share load. The current transient after the TBC is closed is caused by the transient response of the load-division control circuits. After this transient the converters then divide load within the load-division limits of 0 to 0.49 amperes.

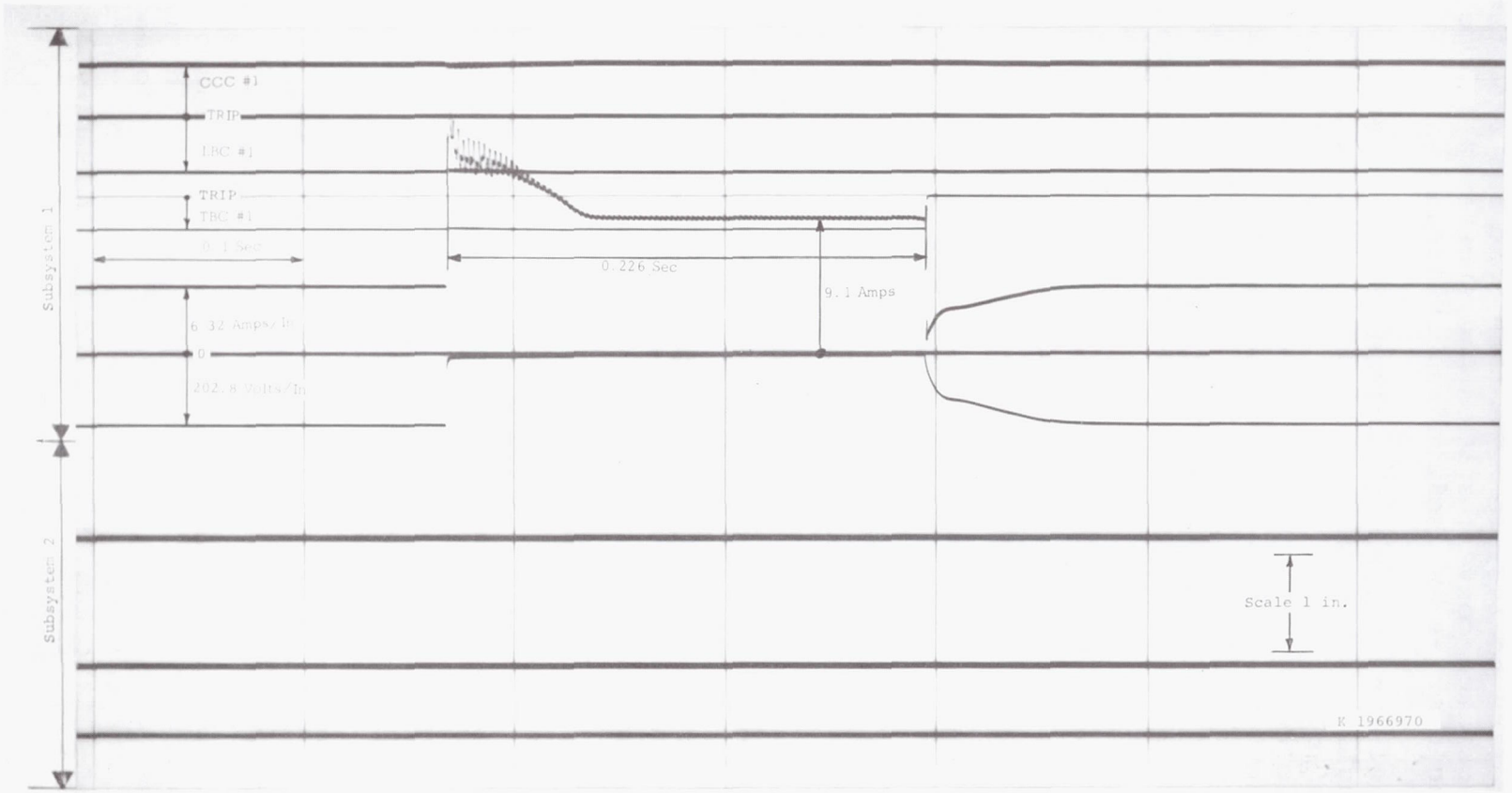


Figure 46. - Converter No. 1 - Isolated, Tie-Bus Fault

Table XIII. - Steady-state Load Division of Automatically Paralleled Converter Systems

Subsystem No. 1		Subsystem No. 2		Difference Current* (Amps)
Voltage (Volts)	Current (I_1) (Amps)	Voltage (Volts)	Current I_2) (Amps)	
152	0.15	152.2	0.02	0.13
151.5	0.50	152	0.50	0
151.5	1.0	152.5	1.25	-0.25
152	2.0	152.5	1.89	0.11
152	2.5	152.5	2.35	0.15
--	4.0	--	4.06	-0.06
152	5.0	152.5	4.90	0.10

* I_1-I_2, Limits: 0 to 0.49 amps

Comparison of the length of time delay TD7 to the required length specified in table XII shows that TD7 in both systems is longer than specified. This is because these oscillograms were taken prior to correcting the converter C/P voltage regulator. The only effect of the longer time delay on system performance is a slightly longer period before the TBC is closed. These tests were therefore not rerun.

Figure 47 shows that the automatic C/P circuits provide the proper contactor sequencing to parallel any converter to a parallel system.

Figures 48 and 49 show the operation of the Dead Tie Bus portion of the automatic paralleling circuits. Figure 48 shows an attempt to automatically parallel to a tie bus which has a voltage potential of between 5 and 130 volts applied to it. In this case, 20 volts was applied to the tie bus and subsystem 1 started by closing CCC No. 1. After the initial startup time delay, the LBC closed and began supplying current to load bus No. 1. Because the tie bus had a potential of 20 volts, the dead-tie-bus circuit prevented the TBC from closing. After 1.9 seconds the TBC was not closed (the end of the oscillogram). Figure 49 is a continuation of figure 48. At the beginning of figure 49 the TBC is

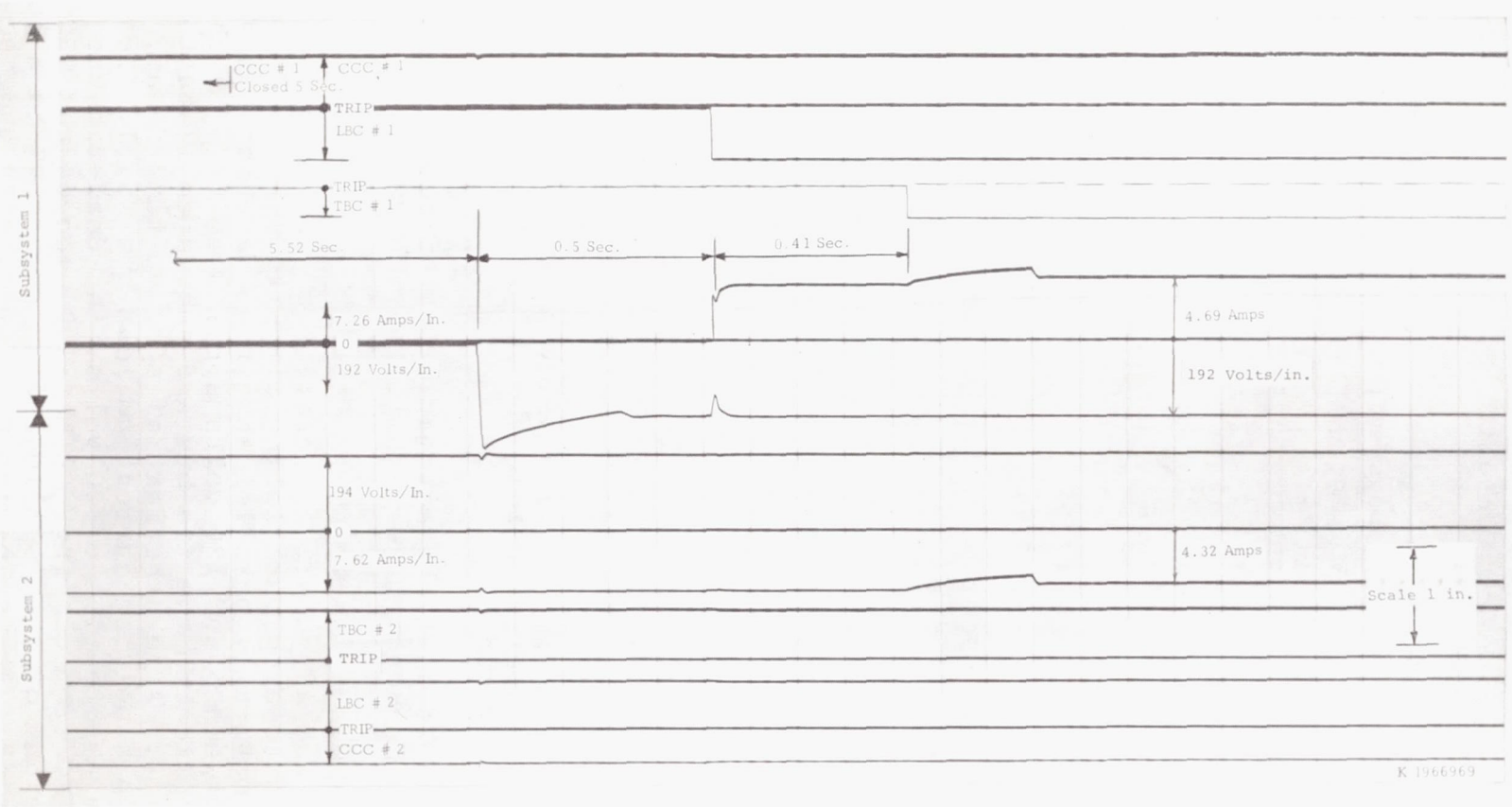


Figure 47. - Automatic Paralleling Converter No. 1 to Converter No. 2

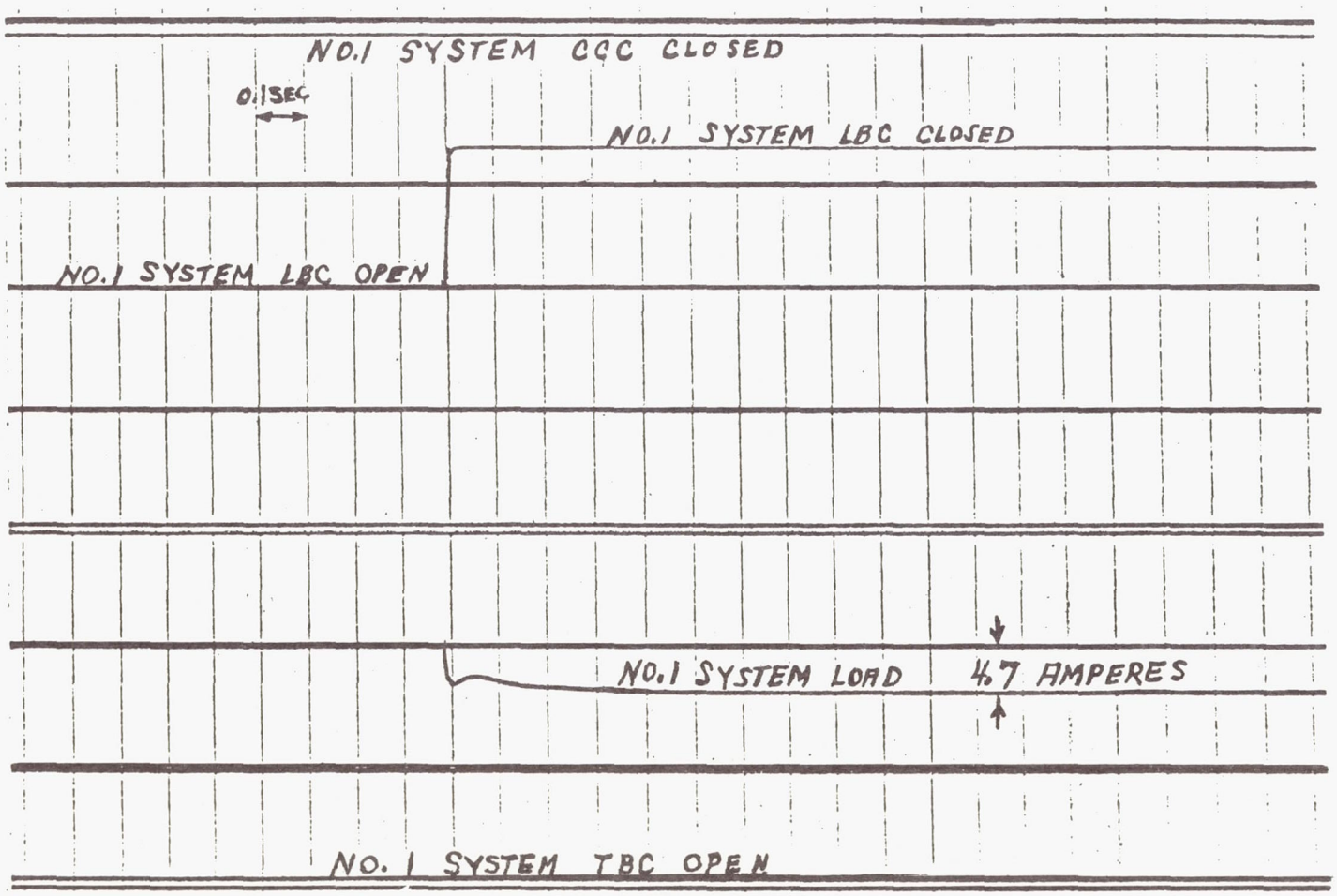


Figure 48. - Dead Tie Bus Protection - No Power Ready Tie Bus Voltage Exists

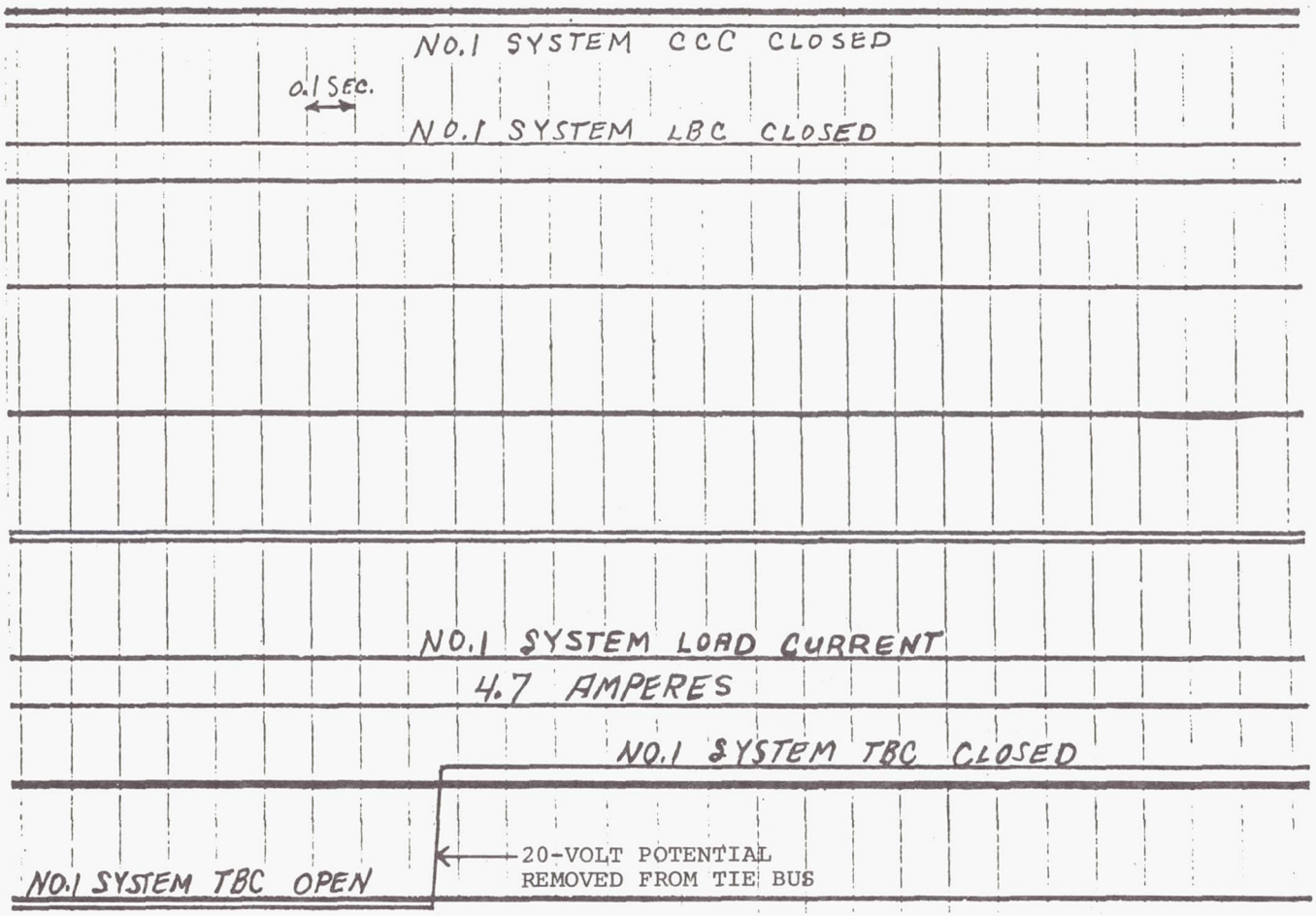


Figure 49. - Dead Tie Bus Protection - Removal of Abnormal Tie Bus Voltage

still not closed. When the 20-volt potential was removed from the tie bus, the TBC immediately closed. Calibration of the dead-tie-bus circuit showed that it would prevent the TBC from closing for any voltage above five volts.

Load-division protection: These tests demonstrated that the load-division protection circuit trips the TBC when the current unbalance falls within the range shown in table XII. Because the calibration of the trip point is dependent on power-supply voltage and the magnitude of the total current being supplied to the system loads, a calibration curve is given in figure 50. The upper portion of figure 50 shows the calibration curves for the two possible directions of circulating current in the LDP circuit. The two schematic diagrams in the lower portion of figure 50 show the test set-ups for achieving the calibration curves. Figure 50 shows that the trip points, shown by the cross-hatched areas, fall well within the established trip range. The effect of variations in power-supply voltage is shown by the bandwidth of the trip range. To show the operation of the C/P circuits, a load-division fault was simulated by opening the load-division control loop within the paralleled converters. Figure 51 shows the result of a load-division fault. The fault is applied at the left edge of the oscillogram, the currents drift apart as shown in figure 51, and the TBC trips after 0.806 seconds, isolating the two converters. Since only two converters are present, one trip effectively makes the load-division control and load-division protection circuits inoperative. To show that both LDP circuits operate, the LDP circuit in subsystem 2 was disabled so that the LDP in subsystem 1 could operate.

The load-division protection circuits sensed the fault conditions and tripped the TBC as required. The type of load-division protection used in these circuits does not provide selective tripping when only two subsystems make up the parallel system. Selective tripping, however, is not necessarily required since opening either TBC effectively isolates the subsystems and renders the load-division control and protection circuits inoperative. "Converter Control and Protection Circuit Design" describes how selective tripping is accomplished when three or more inverters are paralleled.

Differential current (Zone 1): This test demonstrated that faults in Zone 1 isolate a subsystem from the parallel system. (See discussion on differential current protection tests during automatic, single subsystem.) Figure 52 shows that prior to a Zone 1 fault, each converter is supplying approximately two amperes. During the fault, however, converter No. 1 supplies 12.7 amperes to the DP fault while converter No. 2 increases its output current to only about four amperes. Converter No. 1 supplies the total Zone 1 fault current while inverter No. 2 assumes the total system load because the series diode in the DP sensing

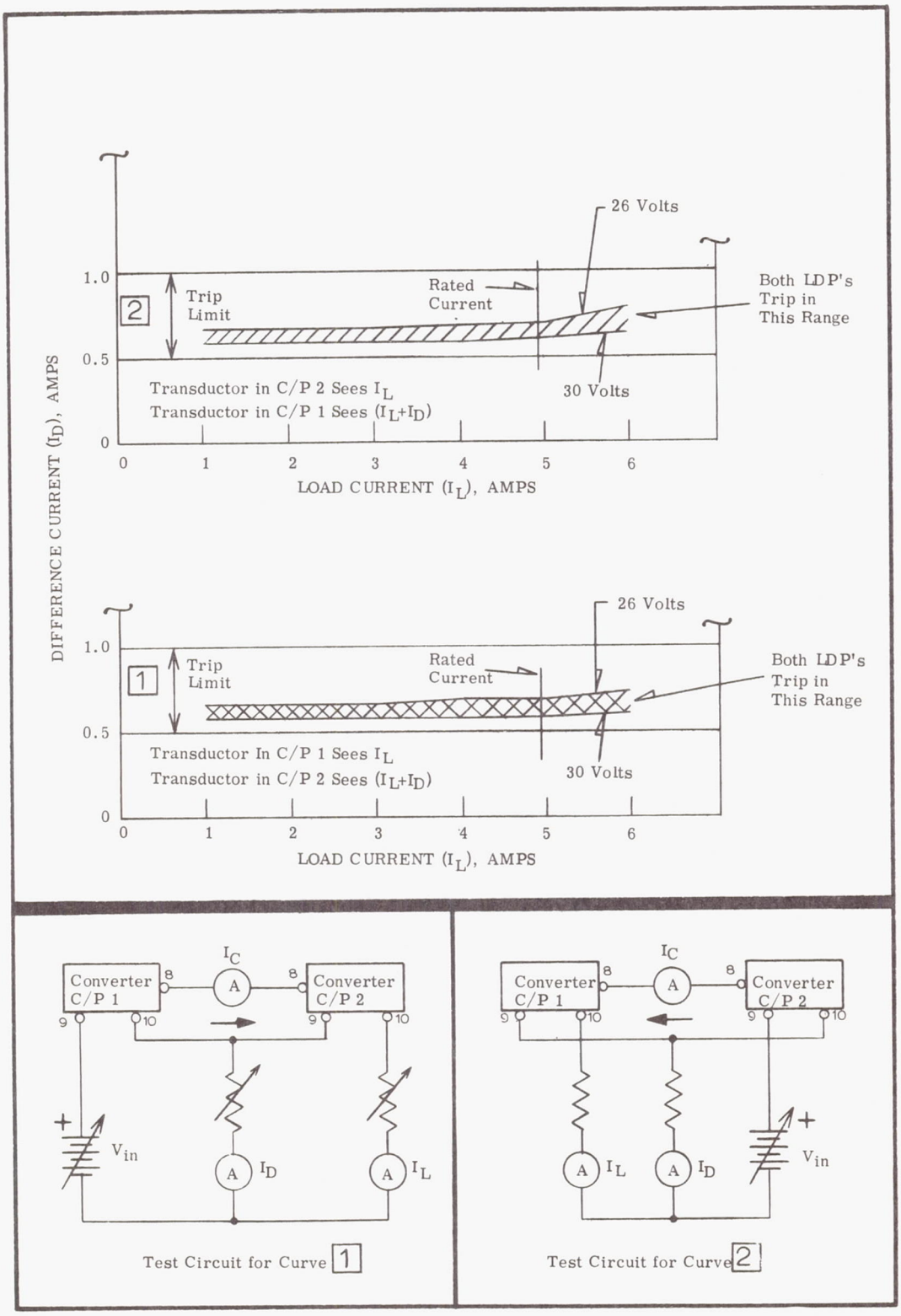


Figure 50. - Characteristics of Load-Division Protection Circuits

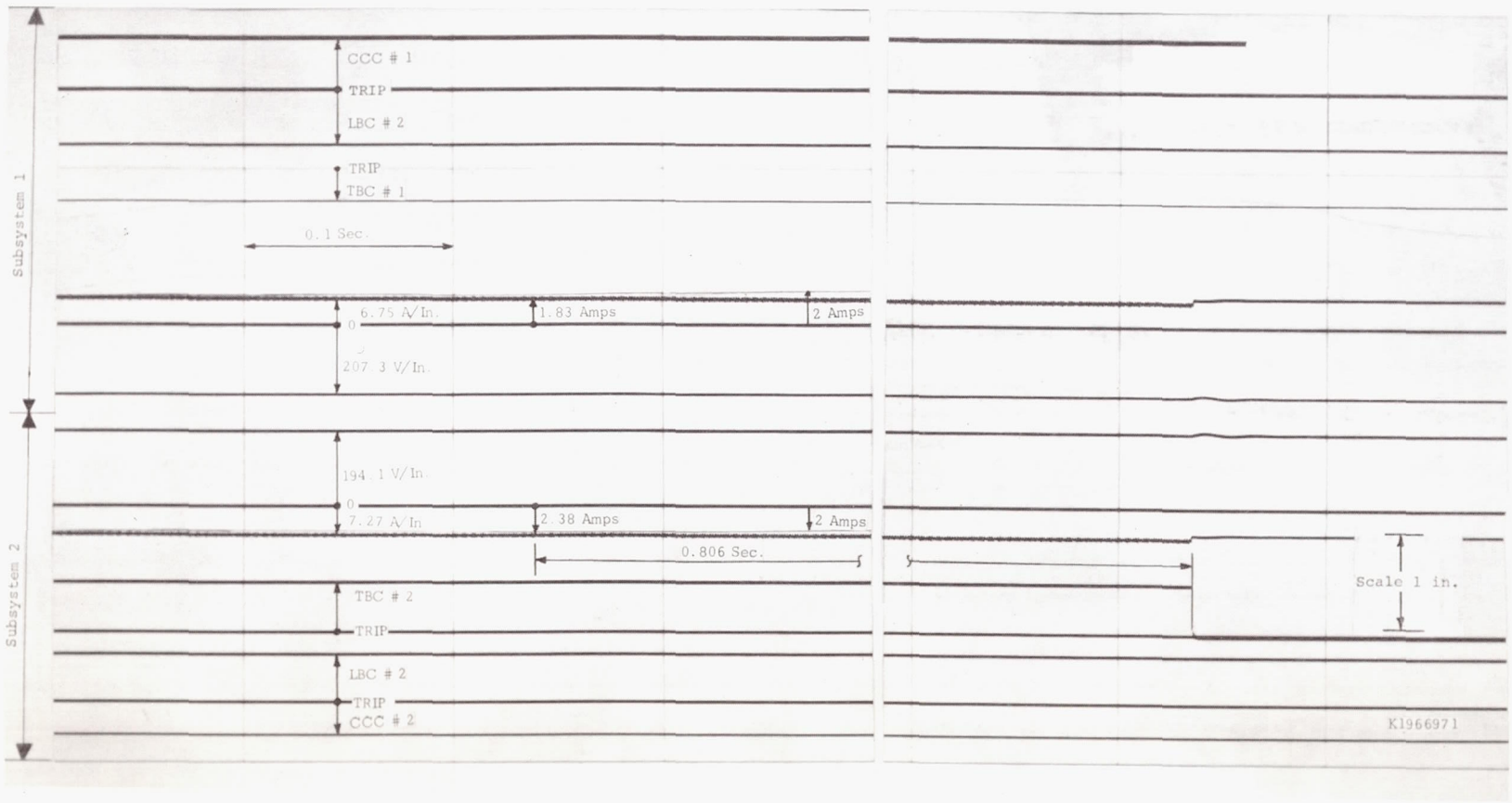


Figure 51. - Parallel Converter System, Open Load-Division Loop, Load Division Protection Test

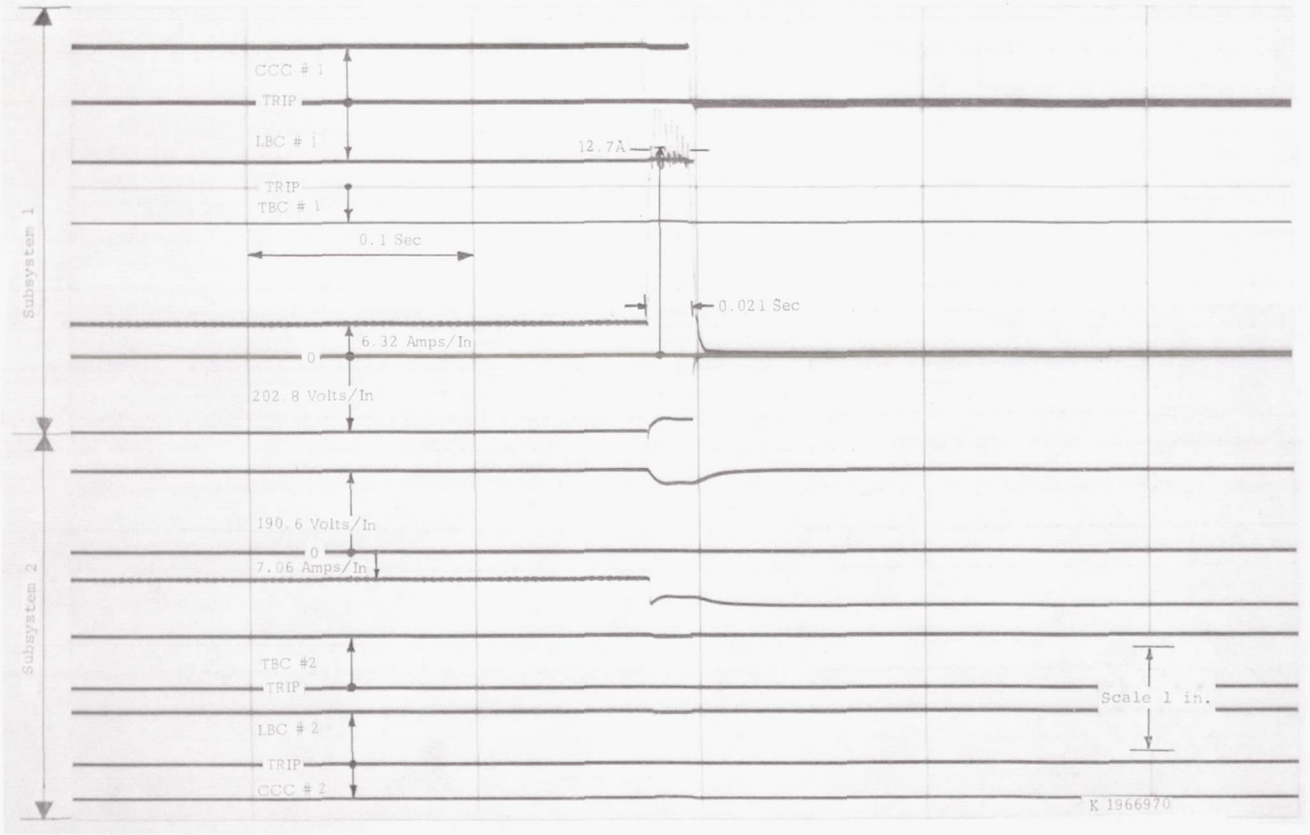


Figure 52. - Parallel Converter System, Zone 1 Fault on Subsystem No. 1

circuit prevents reverse current in Zone 1. After the LBC No. 1 is tripped, converter No. 2 picks up the total system load of about four amperes.

Except for the variation in trip point, the differential current protection circuit performs as required.

Load-bus overcurrent protection (Zone 2): This test demonstrated that the control and protection sensing and logic circuits can locate and isolate an overcurrent fault. Table XII shows the measured trip points of the converter and the tie-bus overcurrent sensing circuits. A load-bus overcurrent fault will cause both overcurrent sensing circuits in a faulted subsystem to have an output; thus, time delays TD4 and TD6 are initiated. Figure 53 shows the system operation for a fault on load bus No. 2. Prior to the fault, both subsystems are operating paralleled and each is supplying current to the system. The fault is applied as evidenced by the sudden rise in current on both converters. After 0.106 second (TD6), TBC No. 1 is tripped. This action removes the fault from the parallel system; hence, converter No. 1 voltage recovers to nominal and its current decreases to the parallel system load (load bus No. 1 in this case). Converter No. 1 continues to feed the fault for an additional 0.338 seconds at which time LBC No. 2 and CCC No. 2 trip. Note that the TBC trips much sooner for load-bus faults in a parallel system than the same fault in a single subsystem (see figure 46). This is because the TBC sensing circuit is activated only in a parallel system; i.e., the tie bus is furnishing current to the faulted load bus. The LBC, however, trips in the same accumulated time (TD4 plus TD5).

This oscillogram shows that the control and protection circuits provide the proper system operation for a load-bus fault.

Tie-bus overcurrent protection (Zone 3): This test demonstrated that a faulted tie bus results in all subsystems operating as isolated power sources. Figure 54 shows the system operation for a faulted tie bus. Note that the operation is the same as shown in figure 47 when a tie-bus fault occurs on a single subsystem.

CONCLUSIONS

This program efficiently and reliably accomplished and maintained automatic paralleling and protection of two or more static inverters and converters. The technology for achieving these functions was developed and the circuits resulting from this technology were verfied by tests on a two-channel parallel system.

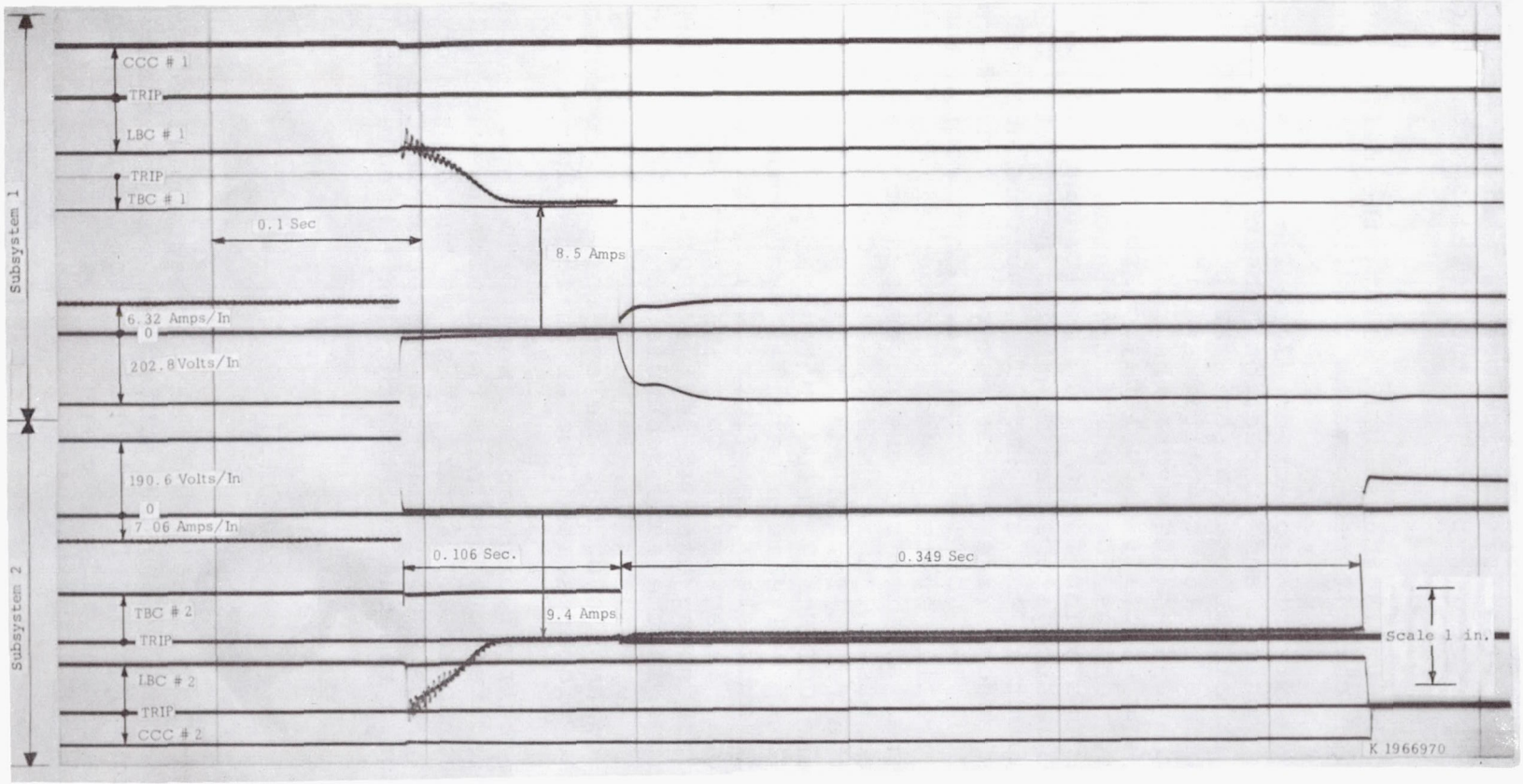


Figure 53. - Parallel Converter System, Fault on Load Bus No. 2

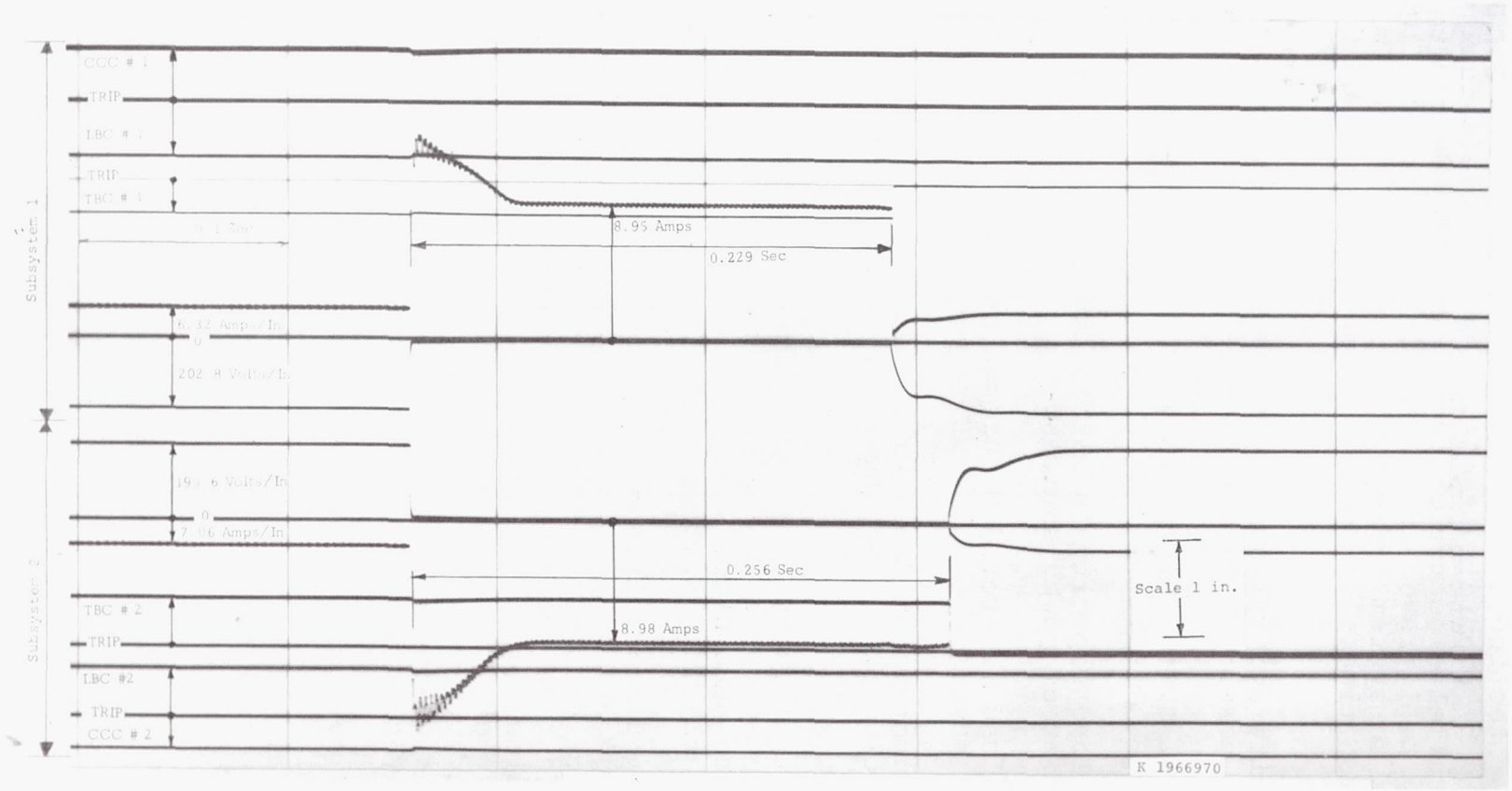


Figure 54. - Parallel Converter System, Fault on Tie Bus

The control and protection circuits can aid in increasing power system reliability by providing the ability to isolate faulty portions of a parallel electric power system. The degree to which reliability is improved is a function of system configuration with respect to system capacity, load power demands, mission objectives, mission time, load priority requirements, and the like.

System capacity and reliability are enhanced by providing a parallel electric power system with the following characteristics.

(1) The total system capacity is provided by several power sources.

(2) System load capacity is maintained with the loss of a predetermined number of power sources.

(3) System load is provided through several load connection points (load busses).

(4) System protection isolates system faults before damage occurs to any portion of the system while maintaining maximum load capacity.

By dividing the system into three zones, it has been possible to evolve an approach to system protection by providing protection for each subsystem. This means that each subsystem can act independently of all others.

The control and protection philosophy was developed by determining the needs of the system. Using the logic diagrams, control and protection circuits were built and tested. The primary goals of extending the control and protection of the parallel electromechanical system to the static power system were achieved. The systems tests showed that the paralleled inverters or paralleled converters can be automatically controlled and protected with little change in performance when compared to the original, manually controlled, paralleled systems.

The means of synchronizing inverters during automatic paralleling provided minimum transient condition on the parallel system. This approach to automatic paralleling can be extended to any inverter with an internal countdown circuit operating from a common frequency reference. The synchronizing circuits can be simplified for parallel inverter systems whenever frequency transients are of little concern.

The parallel converter system required a very small impedance in the load-division control loop. A static, zero-impedance

switch was developed to provide this function. The "contact" drop was reduced from about 1.7 volts to about 0.1 volts. The use of this switch resulted in no increase in current-division error when compared to a mechanical relay or switch. And, the load-division protection circuit provided very close limits on the trip point, with changes in both load current and voltage applied to the control panel (26 to 30-volt range).

APPENDIX

TRANSIENT CHARACTERISTICS OF STATIC CONVERTERS AND INVERTERS

For either isolated or parallel system operation of static converters or inverters, transient conditions occur during which the basic system parameters of voltage, current, and (for ac systems only) frequency exceed their nominal limits. These conditions are caused by the sudden application or removal of large system loads or removal of fault conditions. The transient conditions exist for only short periods and are an inherent characteristic of static converters/inverters and their voltage regulating and load division control circuits. No damage to utilization equipment or the converters/inverters themselves will occur for these conditions and no system protection against them is required.

However, other transient or abnormal conditions of the basic system parameters may occur which are a result of a failure in the basic control circuits. For these conditions automatic system protection must be provided which is capable of distinguishing between a normal system transient condition and an abnormal system condition. This is accomplished by using time delays, in conjunction with the system protection, sufficient to allow transient conditions to occur and steady-state conditions to be reached prior to operation of the protective circuits. The normal transient characteristics of the converter/inverter must be defined in order to determine the length of time delays required.

During the first portion of this contract, system tests were conducted where both static converters and inverters were paralleled under various conditions of initial system load and voltage. From the results of these tests, the transient response characteristics of the converters and inverters were obtained, and the time delays necessary in the control and protection circuits were determined. The results of the above tests are summarized below.

Static converter transient response characteristics. - Three types of tests were conducted on the static converters. Each is discussed below.

(1) The first type of test consisted of paralleling two converters with identical initial loads and output voltages. The tests were run for initial system loads of 0, 25, 50, 75, 100, and 125 percent of rated load.

Review of these data shows that only very slight transients occurred for any of the above test conditions. Voltage changes were less than 5 volts from the initial voltage setting. The time duration was less than 14 milliseconds.

Since the transients caused by the above condition were so slight compared with those of paragraph (2) below, they were not considered in determining the maximum transient response of the static converters.

(2) The second type of test consisted of paralleling two converters with large differences in initial load or applying a large load to parallel converters.

The transients caused by these tests were the most severe obtained. The transients caused are shown in figures 55 and 56.

Figure 55 is the oscillogram of the system voltage and current transient caused by placing rated load on two paralleled, unloaded converters. This produced the most severe transient condition of all the tests conducted. The maximum time required for recovery of the system voltage was 56 milliseconds. A considerable droop of system voltage occurred, reaching a minimum of 96 volts from an initial setting of 153 volts.

(3) The third type of test was to parallel two fully loaded converters with different initial no-load voltage settings. The transient conditions that resulted were negligible compared with those obtained from the test of (2) above and were not considered in determining the maximum system transient response time. Information contained in figure 56 was taken as the maximum time duration of the transients since the transient response characteristic of the static converters is affected most severely by heavy loads.

An additional 14 milliseconds was arbitrarily added to the response time to allow for variations that may occur within the converters and during system operation which may affect the transient response. The maximum response time of the converter is then taken as 70 milliseconds. This value is considered the minimum time delay to be provided for protection circuits that sense abnormal system parameters during transient conditions. The protection circuits will not operate during this time period.

Static inverter transient response characteristics. - Four sets of tests were conducted on the static inverters. Each is briefly discussed below.

(1) The first sequence of tests consisted of paralleling two inverters, each at 100 percent of rated load with the power

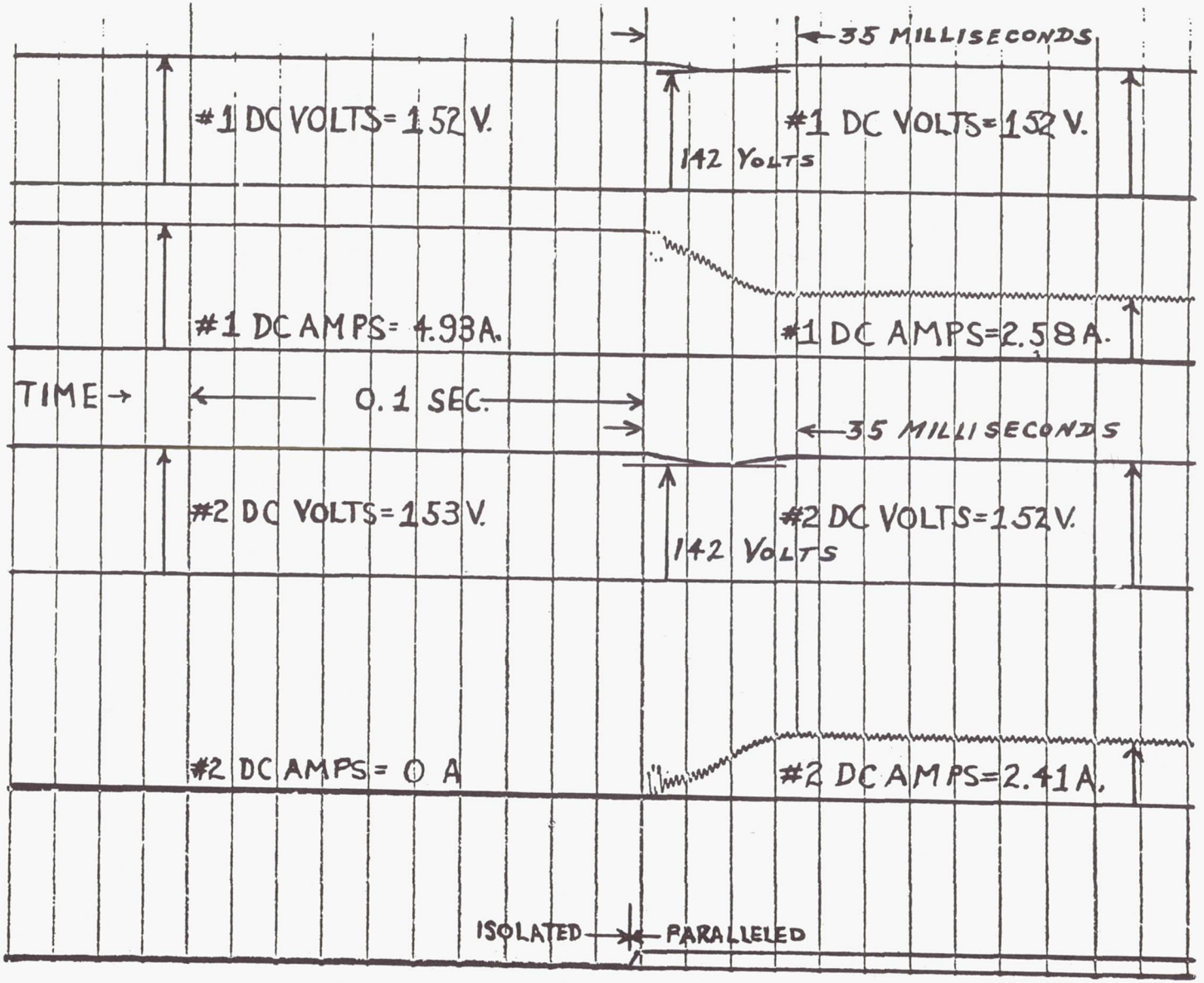


Figure 55. - Oscillogram of the Transient Caused by Paralleling a Loaded Converter with an Unloaded Converter

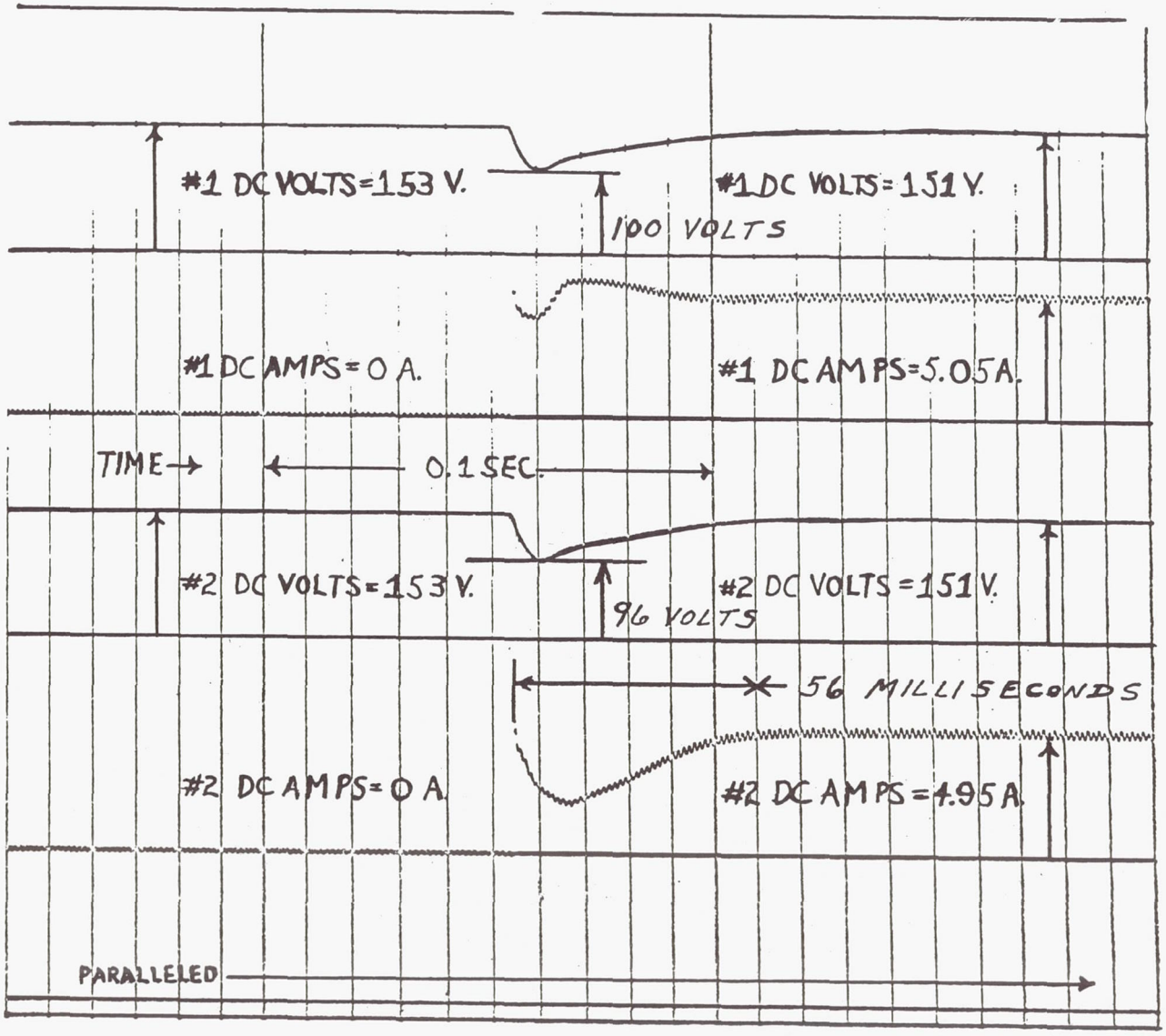


Figure 56. - Oscillogram of the Transient Caused by Placing Rated Load on Two Paralleled-Unloaded Converters

factors of 1.0, 0.75 lagging, 0.9 lagging and 0.9 leading. The transients produced during these tests were negligible and were not considered in determining the transient response of the static inverter.

(2) The second sequence of tests consisted of paralleling inverters with unbalanced loads and suddenly applying loads to paralleled inverters. The maximum current transient produced under these conditions was 50 milliseconds. The transient occurred when an inverter carrying rated load was paralleled to an unloaded inverter. Approximately the same transient was observed when rated load was suddenly applied to two paralleled inverters. In the second case the inverter output voltage dropped from 115 to 114.5 volts. Figure 57 is an oscillogram which illustrates the second case.

(3) The third sequence of tests consisted of paralleling inverters with unequal input voltages, unloaded; and paralleling them with unequal output voltages, loaded with rated current for one inverter (at power factors of 1.0 and 0.75 lagging). The maximum transient occurred at a power factor of 1.0. This transient was 40 milliseconds long.

(4) The fourth sequence of tests consisted of starting a one-eighth horsepower motor with one inverter and then with two inverters in parallel. Figure 58 is an oscillogram which shows the transient caused when one inverter starts a one-eighth horsepower motor. The output voltage in this test dropped initially to 75 percent of its original value. The transient caused was 140 milliseconds long.

Although the fourth test produced the most severe transients, a shorter time delay was used since the loads to be used for demonstration purposes in this program were constant. Except for the motor test, the most severe transient was 50 milliseconds in duration. Therefore, to ensure that system transients have time to decay, a minimum of 80 milliseconds was chosen for all time delays in the inverter system except for protection circuits where no time delays was provided.

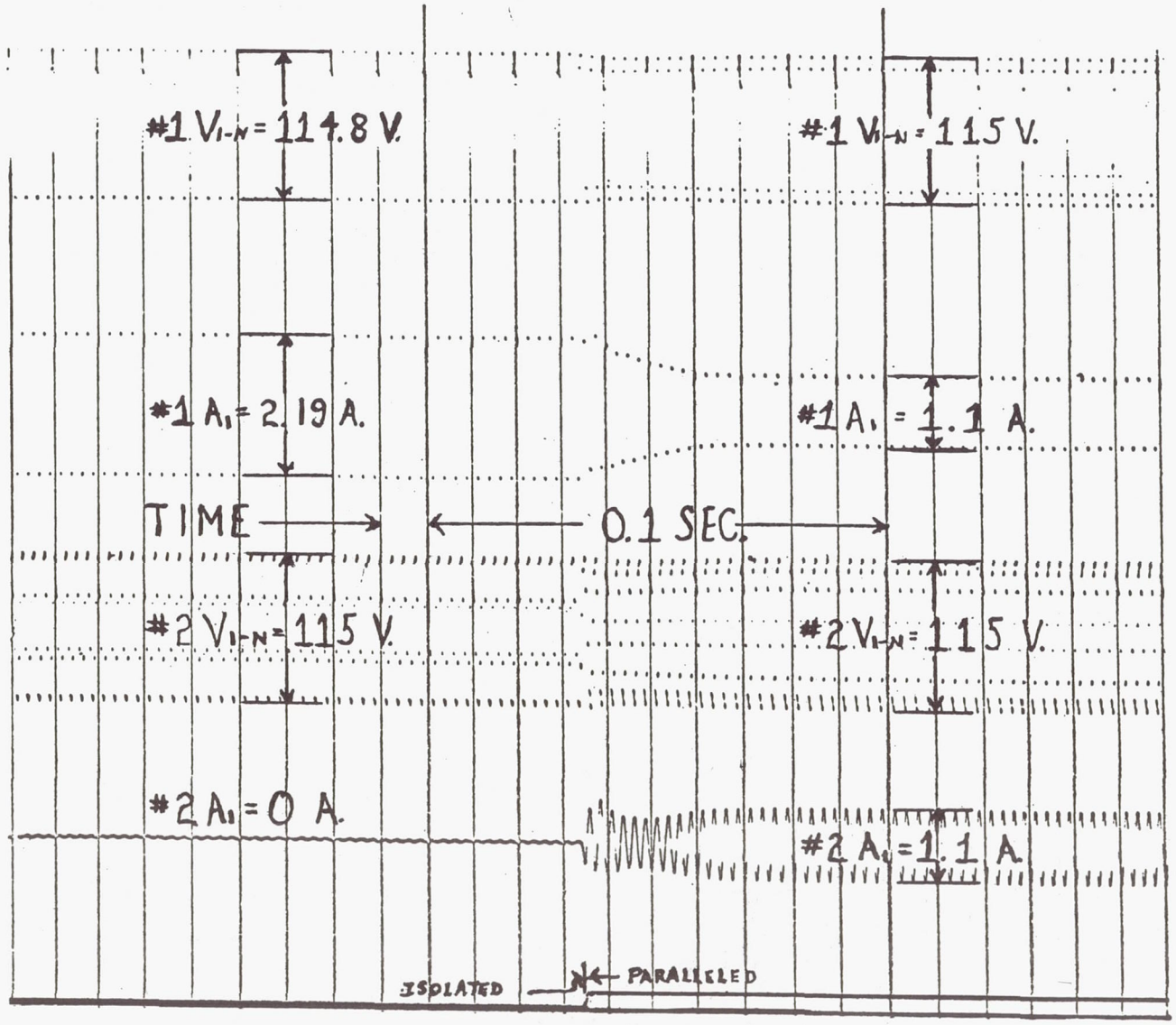


Figure 57. - Oscillogram of the Transient Caused by Paralleling a Loaded Inverter with an Unloaded Inverter

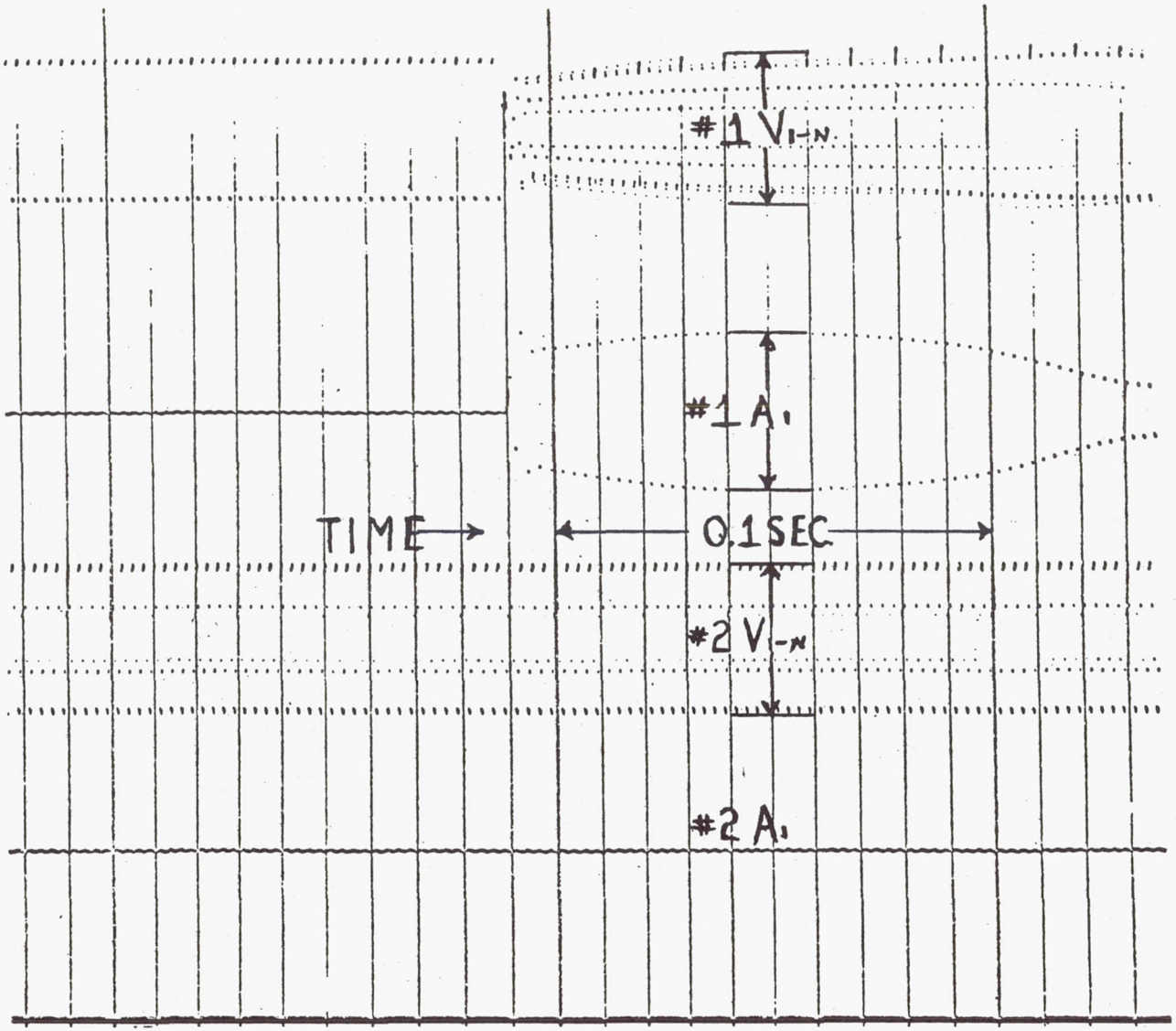


Figure 58. - Oscillogram of One Inverter Starting a 1/8 HP Motor

REFERENCES

1. Corey, P.D.: Methods for Optimizing the Waveform of Stepped-Wave Static Inverters; AIEE CP-62-1147.

2. Kernick, A., J.L. Roof, and T.M. Heinrich: Static Inverter with Neutralization of Harmonics; AIEE Transactions, Part II (Applications and Industry), Vol. No. 81, May 1962, pp. 59-68.

3. Billings, W.W.: Frequency Sensors for Aircraft Power Systems; M.S. (Electrical Engineering) Thesis, University of Pittsburgh, 1961.

4. Milne, A.G.: Transductors and Magnetic Amplifiers; MacMillan and Co., 1957.